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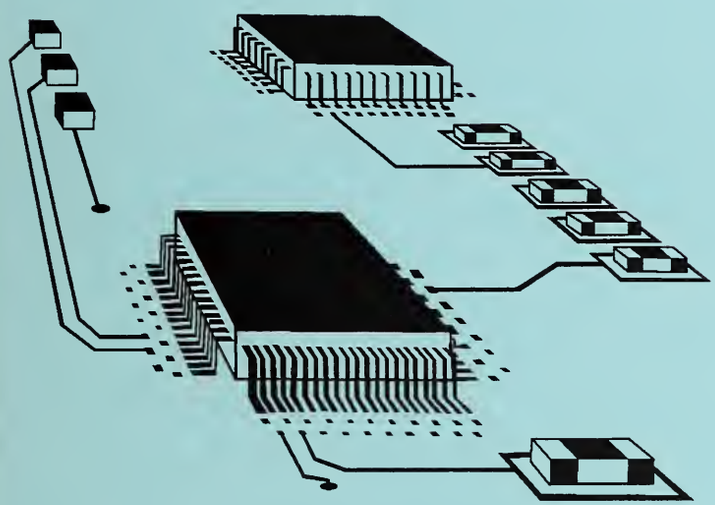
VOLUME II: PRESENTATION MATERIAL

Metrology and Data for Microelectronic Packaging and Interconnection

NISTIR 5520



Results of a joint workshop on Materials Metrology and Data for Commercial Electrical and Optical Packaging and Interconnection Technologies

May 5-6, 1994, Gaithersburg, MD.

Edited by Michael A. Schen
National Institute of Standards and Technology

Sponsored by:

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National Institute of Standards and Technology

Institute for Interconnecting and Packaging Electronic Circuits

Optoelectronics Industry Development Association

Semiconductor Research Corporation

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November 1994

U.S. DEPARTMENT OF COMMERCE
Ronald H. Brown, Secretary

TECHNOLOGY ADMINISTRATION
Mary L. Good, Under Secretary for Technology

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
Arati Prabhakar, Director

COVER ILLUSTRATION

Schematic illustration of contemporary single-chip electronic packaging and interconnection technology consisting of surface mounted components, quad flat-pack semiconductor package, plated through holes and fine-pitch interconnection.

DISCLAIMER

Commercial equipment, instruments, software, materials or services are identified to adequately report the discussions that took place. Such identification does not constitute nor imply recommendation, endorsement, or criticism by the National Institute of Standards and Technology, the Institute for Interconnecting and Packaging Electronic Circuits, the Optoelectronics Industry Development Association, or the Semiconductor Research Corporation.

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APPENDIX C: PRESENTATION MATERIAL

BARRY JOHNSON, MOTOROLA

MOTOROLA

MATERIALS CHALLENGES IN MICROELECTRONIC PACKAGING AND INTERCONNECTION

Barry Johnson
Motorola
Tempe, Arizona

May 5, 1994

MOTOROLA

OUTLINE

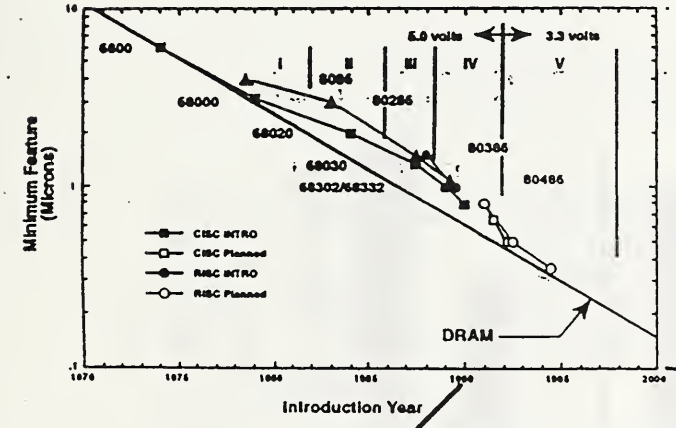
1. MARKET TRENDS
   - SEGMENTS / DRIVING FORCES
   - MPU EVOLUTION
2. IMPACT ON PACKAGING
   - PERFORMANCE ISSUES
   - DESIGN / SIMULATION
3. MULTI-CHIP MODULES
   - SYSTEM'S APPROACH
   - DESIGN GUIDELINES
4. PACKAGING TRENDS

MOTOROLA

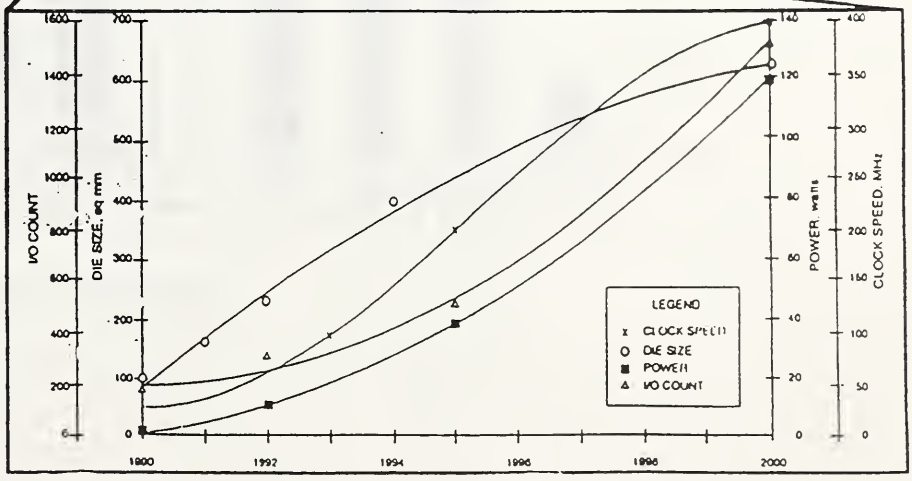
MARKET SEGMENTS / DRIVING FORCES

SEGMENT	DRIVING FORCE
Computer	
Mainframe/Supercomputer	Performance
Workstation/PC	Performance/Cost
Communications	
Fixed	Cost
Mobile	Size, Cost
Space	Performance, Size, Weight
Automotive	
Body	Cost, Size, Weight
Powertrain	Performance, Cost, Size, Weight
Electric Vehicle	Performance, Cost, Weight
Industrial	
Instrumentation	Performance, Cost
Power Control	Performance
Consumer	
Fixed	Cost
Portable/Hand-Held	Cost, Size, Weight

MICROPROCESSOR CIRCUIT TRENDS



IMPACT ON PACKAGING



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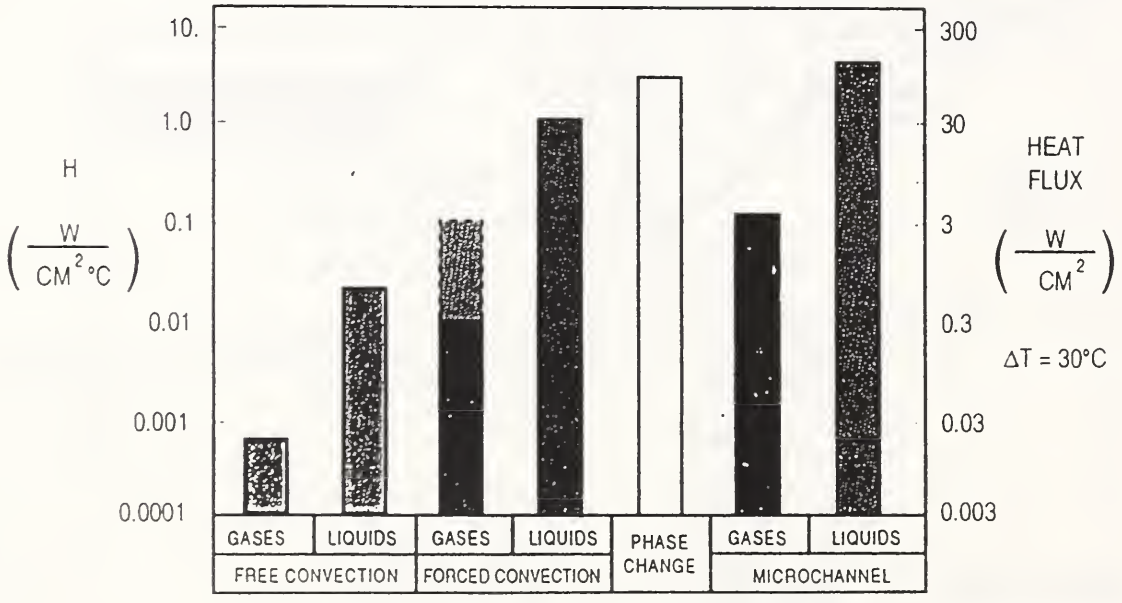
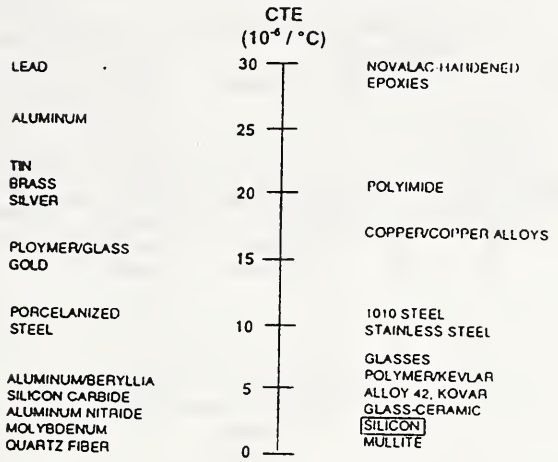
IMPACT ON PACKAGING

- DOWNSCALING
  - HIGHER PINCOUNT / INTERCONNECT DENSITY
  - PACKAGING TO MIMIC CHIP TECHNOLOGY
- IMPROVED MATERIALS
  - GREATER HEAT DISSIPATION
  - BETTER MECHANICAL CHARACTERISTICS
  - HIGHER POWER DISTRIBUTION
  - TRANSMISSION LINE BEHAVIOR
  - INTERFACIAL INTEGRITY
- COST / PERFORMANCE TRADE-OFFS
- ELECTRONIC DESIGN AUTOMATION
- SYSTEM'S APPROACH
- HIGHER RELIABILITY



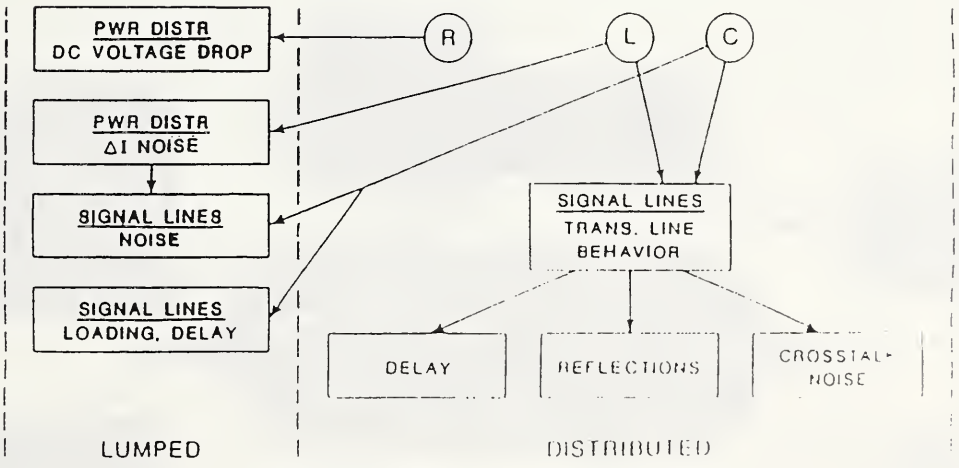
REF: MAHALINGAM (MOD.)

COEFFICIENT OF LINEAR THERMAL EXPANSION OF PACKAGING MATERIALS



$$\sigma = f(\Delta\alpha, \Delta T)$$

$$N_f = f(\Delta\alpha\, \Delta T)^m$$



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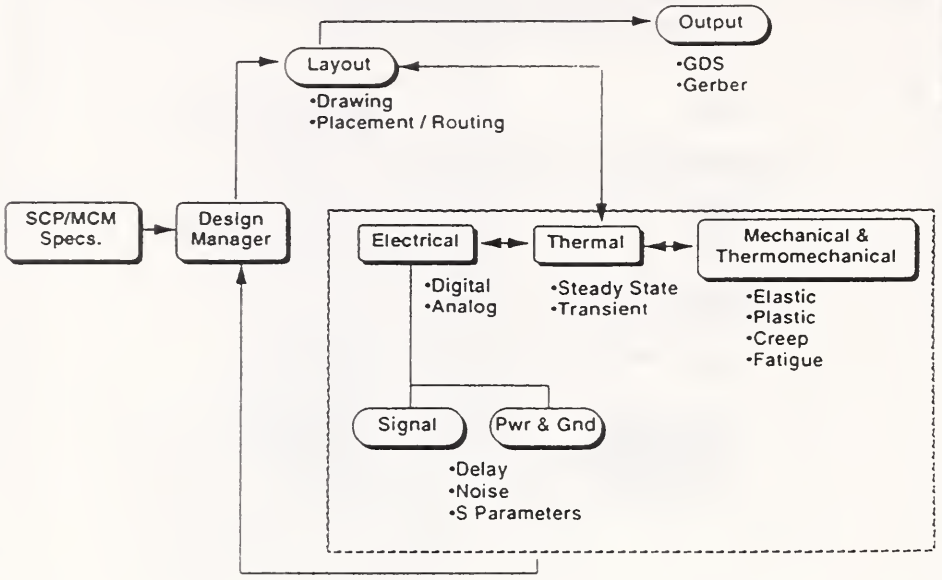
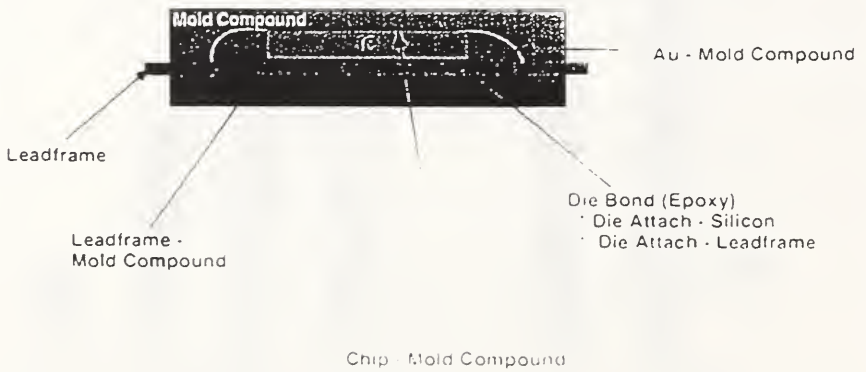
Interactive Design / Simulation



MOTOROLA — Core Technologies

Interfaces In Conventional Packages



MOTOROLA

Core Technologies

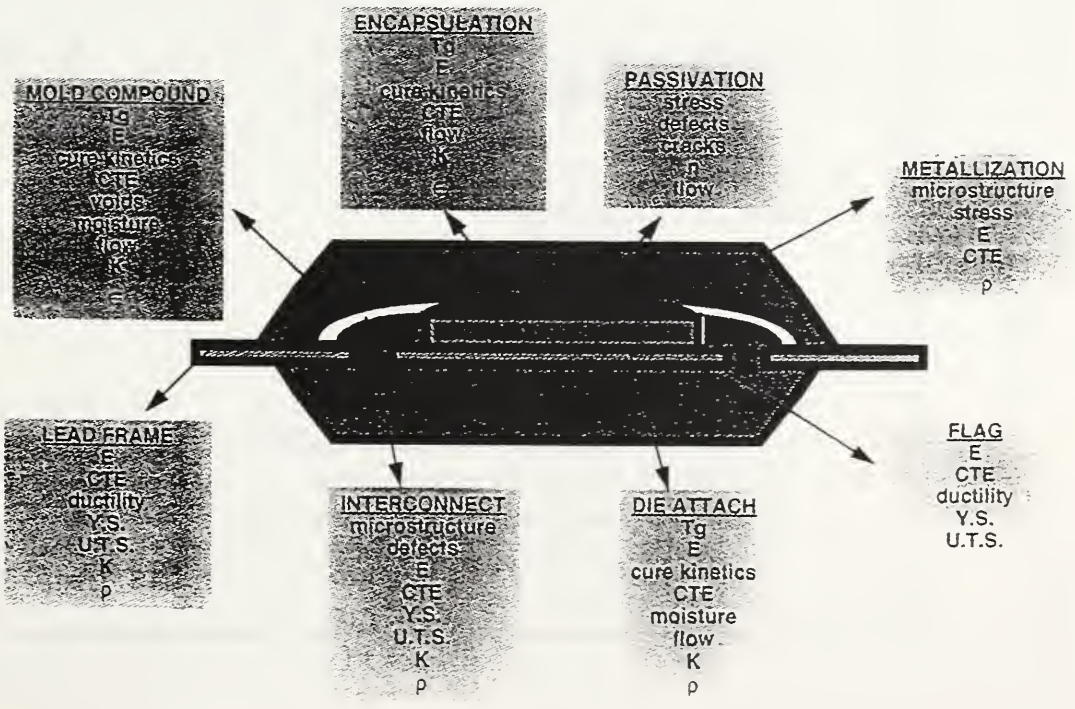
PERFORMANCE CHARACTERISTICS

ELECTRICAL	
• DC VOLTAGE DROP	$V = f(R)$
• ΔI SWITCHING NOISE	$\Delta I = f(N, L, di/dt)$
• PROPAGATION DELAY	$t_d = f(l, \epsilon^{1/2})$
• REFLECTION NOISE	$R = f(Z_o, R_L)$
• CROSSTALK	$K (F.E.) = f(\epsilon)$
• ATTENUATION	$A = f(R, \gamma, TAN\ \delta)$
• DISPERSION	$D = f(\epsilon)$
THERMAL	
• THERMAL RESISTANCE	$\theta_{JC} = f(K, l, A)$
	$\theta_{CA} = f(h_c, e, A)$
• THERMAL CAPACITY	$C_{Th} = f(Cp, \rho, V)$
MECHANICAL	
• STRESS	$\sigma = f(P, E, \eta, Y.S., UTS, T, s)$
• STRAIN	$s = f(P, \sigma, Y.S., UTS, T, \sigma)$
• CREEP	$\dot{C} = f(\sigma, T, dP/dt)$
• FATIQUE	$F.S. = f(\sigma/s, N)$

MOTOROLA

Core Technologies

MOLDED PLASTIC PACKAGE



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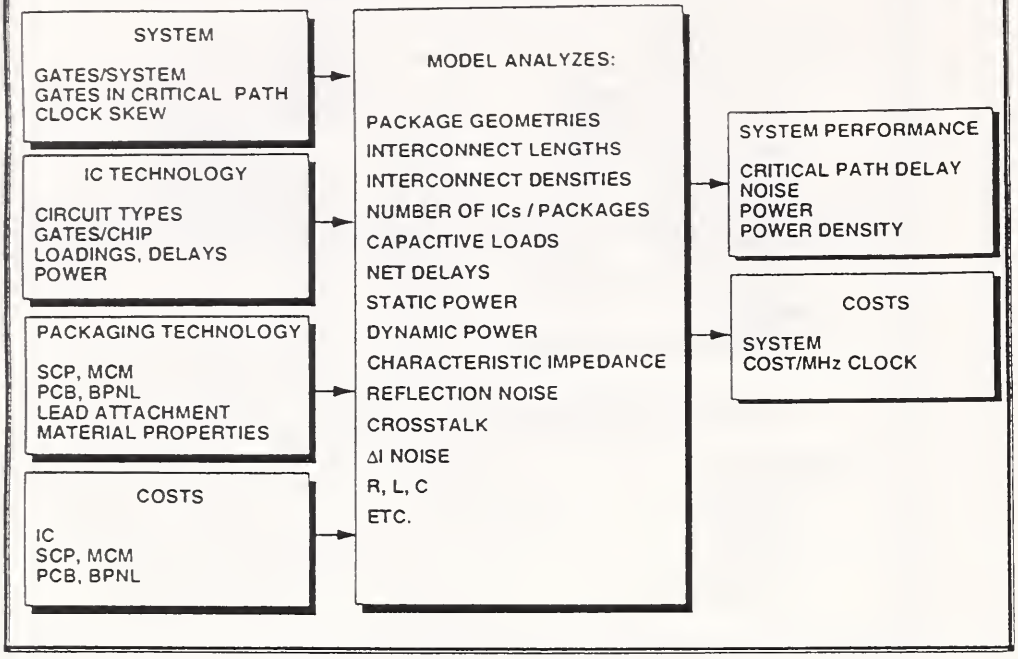
SYSTEM PERFORMANCE MODEL



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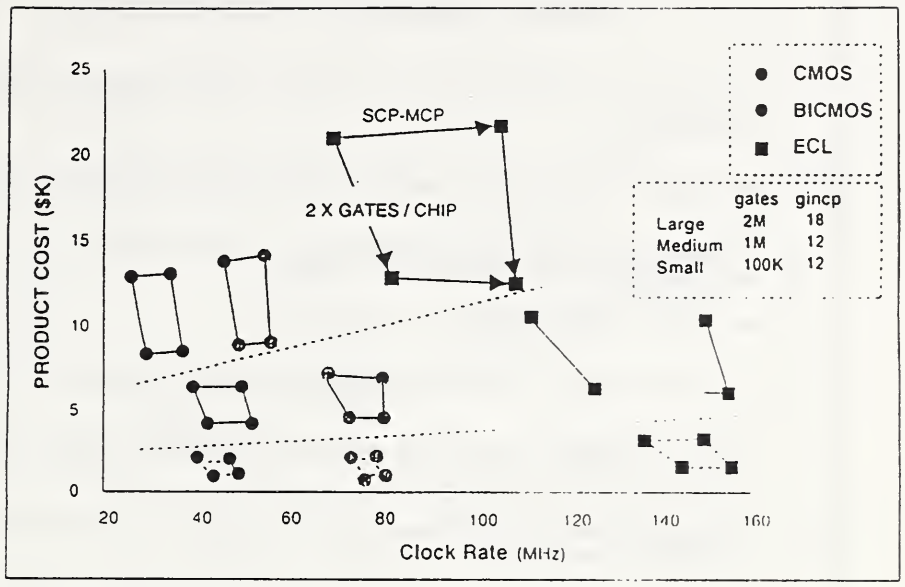
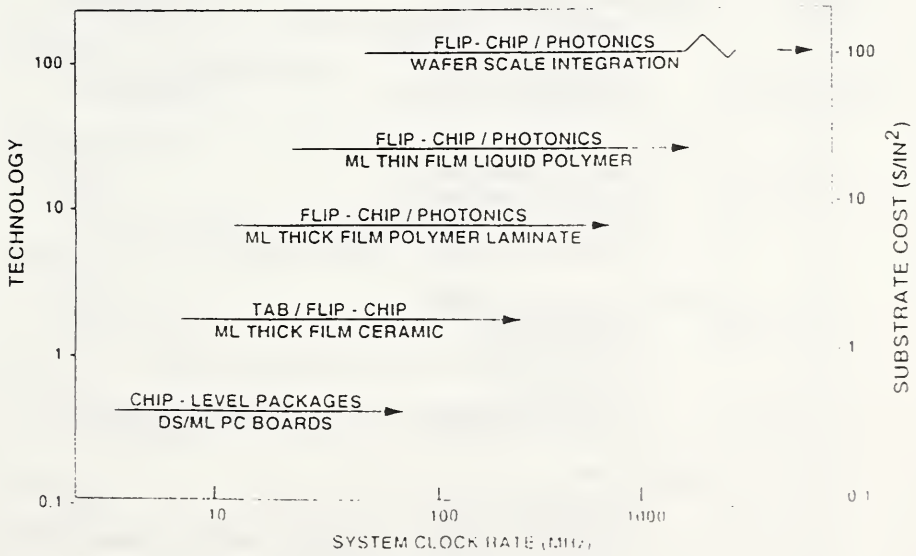
SYSTEM PERFORMANCE ENHANCEMENTS

- ARCHITECTURE — 10 - 100X
  - PARALLEL PIPELINED HARDWARE
  - SOFTWARE
- BASIC TECHNOLOGIES — 2 - 10X
  - LEVEL OF INTEGRATION
  - IC GATE DELAY/DRIVE CAPABILITY
  - PACKAGING DENSITY
- IMPROVEMENTS WITHIN TECHNOLOGY — 2 - 5X
  - CHIP/PACKAGE MATERIALS
  - NUMBER OF CHIPS PER PACKAGE
  - REDUCED PROPAGATION DELAY/NOISE



CIRCUIT AND PACKAGING COSTS VERSUS CLOCK RATE



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DESIGN GUIDELINES FOR HIGH PERFORMANCE PACKAGING

1. SPACE INTEGRATED CIRCUITS AS CLOSELY AS HEAT REMOVAL TECHNIQUES ALLOW.
2. PARTITION HEAT REMOVAL AND ELECTRICAL INTERCONNECT PATHS.
3. INTERCONNECT CIRCUITS WITH HIGH ASPECT RATIO SIGNAL LINES PATTERNED IN HIGH CONDUCTIVITY METAL.

   MAXIMIZE CROSS-SECTION OF POWER LINES.
4. SEPARATE SIGNAL LINES AS FAR APART AS WIRING LAYERS ALLOW.
5. SEPARATE SIGNAL LINES FROM GROUND PLANES WITH THICK LAYER OF LOW K DIELECTRIC MATERIAL.

   SEPARATE POWER AND GROUND LINES/PLANES WITH THIN LAYER OF HIGH K DIELECTRIC MATERIAL.
6. DESIGN IN TESTABILITY AND REPAIRABILITY AT ALL STAGES OF ASSEMBLY.

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MULTI LAYER MCM SUBSTRATES

INTERCONNECTS
- LOW ELECTRICAL RESISTIVITY (Cu = 1.7 MICRO OHM-cm)
- FINE LINE PATTERNABILITY
- LOW STRESS
- ADHESION
- LOW DIFFUSION KINETICS

SURFACE LAYERS
- LOW CTE (Si = 2.6 PPM/C)
- DIELECTIC CONSTANT < 6
- DIMENSIONAL STABILITY, < 0.2%
- PROVIDE RELIABLE VIAS AND PLATED-THROUGH-HOLES
- WITHSTAND ASSEMBLY TEMPERATURES (UP TO 600C)

INTERLEVEL DIELECTRICS
- NONCORROSIVE
- GOOD ADHESION
- LOW FILM STRESS AND HIGH CRACK RESISTANCE
- PLANARIZING
- DIELECTRIC CONSTANT < 3 FOR SIGNAL DISTRIBUTION
- DIELECTRIC CONSTANT >> 3 FOR POWER DISTRIBUTION

PASSIVATION
- DIMENSIONAL STABILITY
- LOW STRESS AND HIGH CRACK RESISTANCE
- ADHESION TO MULTIPLE MATERIALS - METALS, OXIDES, NITRIDES, ETC
- CHEMICALLY INACTIVE INTERFACES
- MOISTURE AND HEAT RESISTANCE
- HIGH THERMAL CONDUCTIVITY

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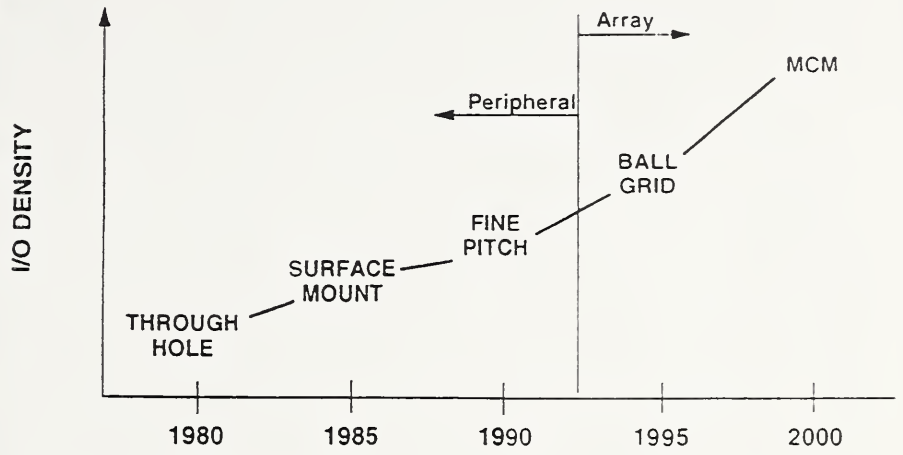
INTERCONNECT EVOLUTION



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MARKET SEGMENTS / PACKAGING TRENDS

SEGMENT	CURRENT	1998/99
Computer		
Mainframe/Supercomputer	Array TH/SM, MCM	Array SM, MCM
Workstation/PC	Peripheral SM	Array SM, MCM
Communications		
Fixed	Peripheral TH/SM	Array SM
Mobile	Array SM	Array SM, MCM
Space	TH/SM	MCM
Automotive		
Body	TH/SM	SM
Powertrain	Peripheral TH/SM	SM, MCM
Electric Vehicle		Hi Power MCM
Industrial		
Instrumentation	Peripheral TH/SM	Peripheral SM
Power Control	Power MCM	Hi Power MCM
Consumer		
Fixed	Peripheral SM	SM, MCM
Portable/Hand-Held	Peripheral TH/SM	

Paul Haugsjaa, GTE Laboratories

Emerging Applications for Low-Cost Optoelectronics

Paul Haugsjaa

GTE Laboratories Incorporated
Waltham, Massachusetts

May 5, 1994

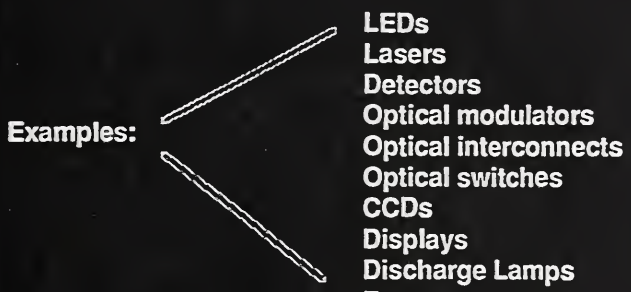
GTE Laboratori

Scope of Presentation:

- What is optoelectronics?
- Drivers for technology today
- Important cultural forces
- Evolving technological needs
- Growth areas of OE utilization
- Associated challenges to be met

Optoelectronics:

The technology of the interface between the realms of electronics and of light



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Technology Drivers

- Grand problems
  - — Cancer, immune system, genetics
  - — Weather
  - — Unified physical theory
  - — World economy, etc.
- Improvement in life standards
  - — More of the same - world-wide - means costs must be reduced
  - — Advances dictate strong cost reductions

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Evolving lifestyles - a search for:

- Greater productivity
- Free time
- Instant information /entertainment
- Ubiquitous communications
- Low-cost, safe, reliable transportation
- Better medical care
- Improved personal security

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Evolving Technological Needs

- Personal Communications System (PCS)
- Seamless information network
- Video transport to personal nodes
- Increased computer processing power
- Large, portable, high resolution displays with touch screens
- Low-cost, portable, high resolution printers
- Computer assisted transportation - control, collision avoidance, positioning, routing

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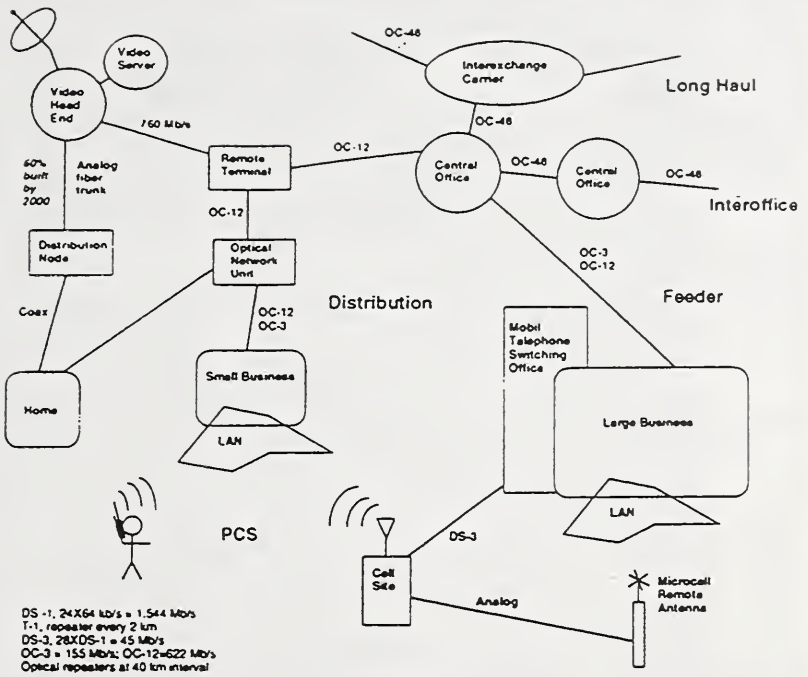
Evolving Network Topology



Evolving Areas of OE Utilization

- ◇ LAN development - > 50% will be wireless
- ◇ Home information network - possibly separate from LAN -- Information appliances
  - — Audio, video, banking, home control, PCS
  - — High speed facsimile
- ◇ WAN development
  - — Extension of optical LAN (latency an issue)
  - — ATM cell traffic carried by SONET transport

Evolving Areas of OE Utilization (Cont.)

- Telecommunications
  - — Video dial tone service
  - — Optical fiber access to network moving nearer the home and into businesses
  - — Homes may have customer owned optical fiber terminals
- Mobile Telecommunications
  - — Optical fiber feeders to MTSOs and cell sites
  - — Optical fiber provides analog links to remote antenna sites

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Evolving Areas of OE Utilization (Cont.)

- Communications distribution
  - — Remote optical terminals and pedestals
    - ° Hostile environment
    - ° Power is an issue
- Vehicular applications
  - — Optical data buses in ships, planes and cars
  - — Optical sensors (gyros, pressure, fluid level, temperature, distance, etc.)
  - — Laser range finder, IR vehicle roadway positioners, smart highway systems

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Evolving Areas of OE Utilization (Cont.)

- Memory / data-storage systems
  - — 2 hr movie needs about 43 Gb (<10 s at OC-12)
  - — Read / write / erase - array enhanced
- Processor interconnects
  - — Multiprocessor cluster connection to arrays of direct access storage devices
  - — Eliminate the bottleneck of slow, interference prone electronic interconnects
  - — Software bottleneck with conventional processor architectures calls for new approaches with high bandwidth interconnects

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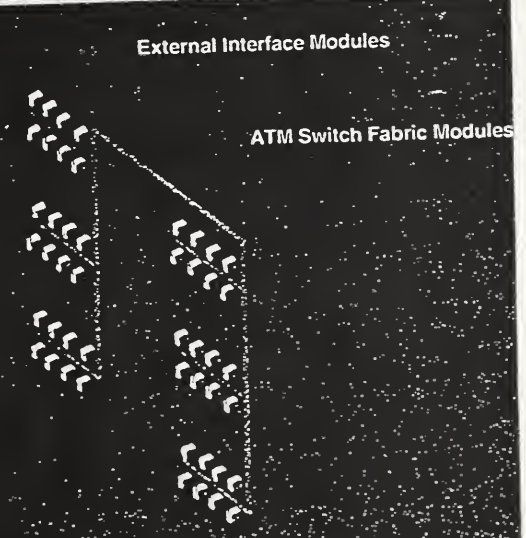
ATM Switch Interconnections

- Optical backplane required
- 16 × 16 1.2 Gb/s ATM requires back plane with over 200 Gb/s capacity
- If assume:
  - — 1 Gb/s on each fiber
  - — 5 fiber module
- 100 fibers = 4100 wires at 50 Mb/s



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Evolving Areas of OE Utilization (Cont.)

- Transparent optical networks - a distant dream?
  - — PICs, WDM components
  - — Optical switching
- OE Sensor Improvement
  - — IR Imaging (plant tissue and textiles)
  - — Absorption (medical, environmental, air quality, process control)
  - — Compact laser scanners - laser arrays
  - — Optical fiber gyros

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Evolving Areas of OE Utilization (Cont.)

- Printers (electrophotographic)
  - — low-cost short wavelength laser diodes and LED optical sources (arrays)
  - — No current US supplier
- Displays
  - — Flexible and portable for digital appliances applications
  - — Integrate drive electronics and display

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Evolving Areas of OE Utilization (Cont.)

- **Metrology and Inspection**
  - **— Improved optical sources**
  - **— Videometrics**
  - **— Higher resolution CCD arrays**

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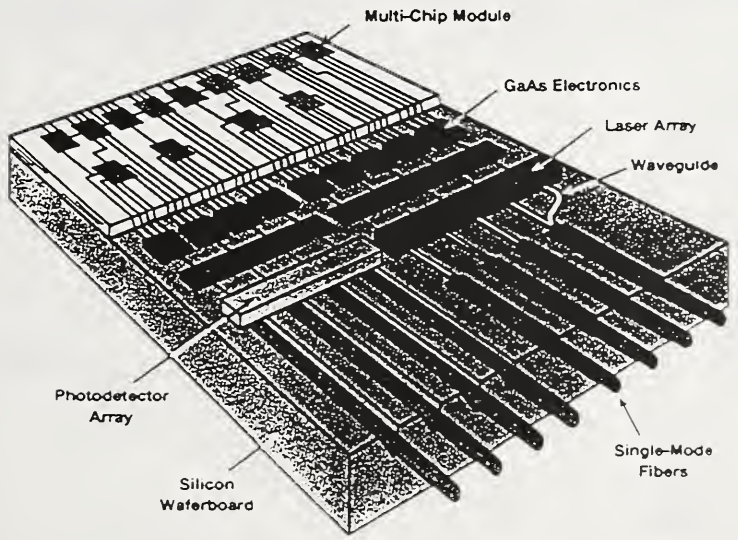
Silicon Waferboard

Silicon Waferboard is an approach that utilizes silicon as a platform for hybrid integration of optoelectronic, electronic, and optical components



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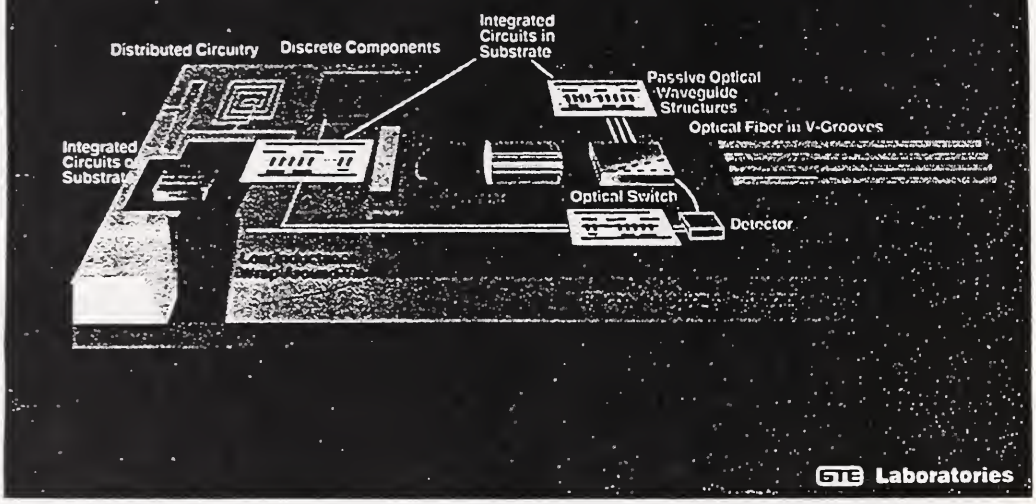
Silicon Waferboard Example



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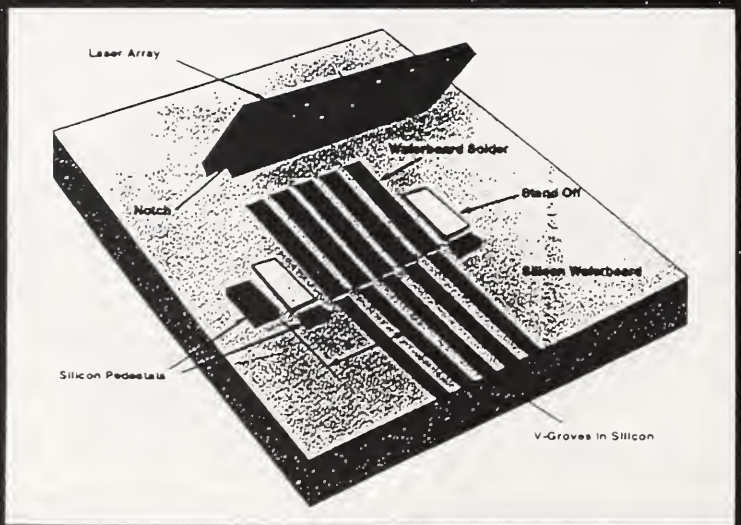
Laser Passive Alignment on Silicon Waferboard



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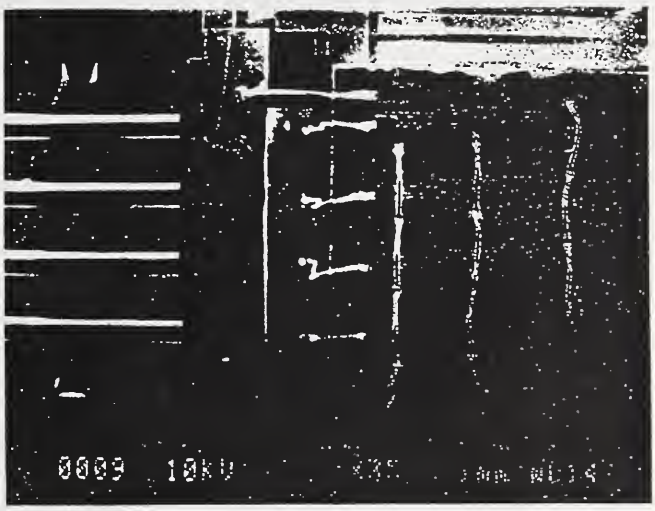
4-Channel Silicon Waferboard Transmitter

- Passive alignment to SM fiber (~7%)
- Array format
- <-29 dB (1GHz) crosstalk
- > 1.4 Gb/s bandwidth



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Challenges for Consideration

- Robotic control
  - — Placement accuracies < 1 μm
  - — Sensitive tactile sensors
  - — High resolution machine vision
- Improved accuracy and precision of submicron measurements over large distances
- Polymer coatings for reliable environmental protection
- New glass hosts for 1.3 μm optical waveguide amplifiers

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Challenges for Consideration (cont.)

- Materials for green and blue LEDs and lasers for optical storage, printers, and displays
- Better polymers for passive and active optical components
  - — Optical couplers
  - — Mode transformers
  - — Optical switches
  - — Optical modulators
  - — Optical memory media

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Challenges for Consideration (cont.)

- Large-area, thin-film process control for uniformity
- Extrusion processes and materials for polymer film deposition over large areas (36 in x 36 in)
- Lateral deposition and epitaxial growth control techniques
- Integrable optical isolators
- Materials and processes for VCSELs and other efficient, long-wavelength lasers and improved MSM detectors

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Challenges for Consideration (cont.)

- Improved resolution CCDs and IR sensors
- Advancements in chemically sensitive OE sensors
- Improved materials and process control techniques for polarization insensitive waveguide switches
- Improved techniques for fabricating good optical switches with moderate (50 - 100 ns) switching speeds

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Grand Challenge:

Reduce the costs involved in fabricating and particularly packaging optoelectronic components to allow continued improvement in our quality of life and the health of our economy.

A Difficult Job -

- Broadly multidisciplinary problems
- National infrastructure for packaging is shrinking
- Team work is the answer

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CHE-YU LI, CORNELL UNIVERSITY

Materials Metrology and Data for Design, Manufacturing, and Reliability Analysis

Che-Yu Li
Electronic Packaging Program
Cornell University

Outline

- Applications and Road Map
- Properties and Data Needs
- Measurement Approaches
- Conclusions and Challenges

Road Map Trends

- Low Cost
- Higher Performance (frequency)
- Low Voltage
- High Junction Temperature
- Mixed Signals

Packaging Trends

- Single Chip:
  - Flip chip
  - Ball grid array
- MCM:
  - Known-good die (Pressure engaged contacts)
- PWB and Flex:
  - Direct chip attach
  - Thin films
  - Early failure sites
- Electrical/Optical Interconnect:
  - Low cost coupling waveguides

- Short cycle time
- Design and simulation
- Properties and data needs

Typical Properties and Data Needs

Electrical:	Dielectric properties Conductivity Contact resistance
Thermal:	CTE Thermal conductivity
Mechanical:	Modulus Flow stress Fracture toughness creep-fatigue Adhesion Early failure sites

Typical Properties and Data Needs (continued)

Optical:

- Refractive index
- Attenuation
- Dispersion
- Coupling loss
- Error rate

Chemical/Physical:

- Permeability, Diffusivity
- Moisture absorption
- Surface tension
- Wettability

Measurement Approaches

- Atomic/molecular level
- Component/sub-component level
- Module/assembly level
- Statistical significance (6σ) (processing, reliability)

Atomic/Molecular Level Examples

- Polyimide/polyimide interdiffusion and adhesion

Component or Sub-component level

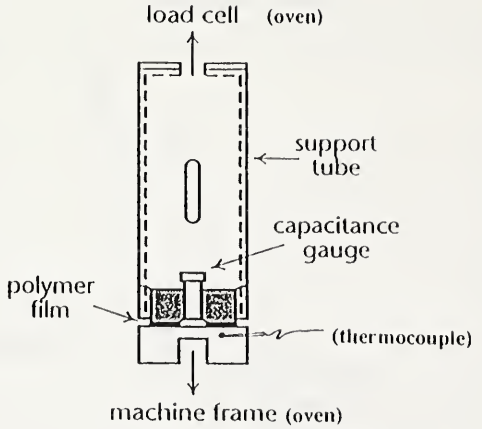
- CTE and modulus of thin polymer films
- Adhesion and residual stress in thin film metallizations
- Creep-fatigue in solder joints
- Contact resistance
- Dielectric properties of thin films

Module/Assembly Level Examples

- Thermal and Residual Stresses in Assemblies (Moiré techniques)
- Early Failure Sites in PWB's (LATEST)

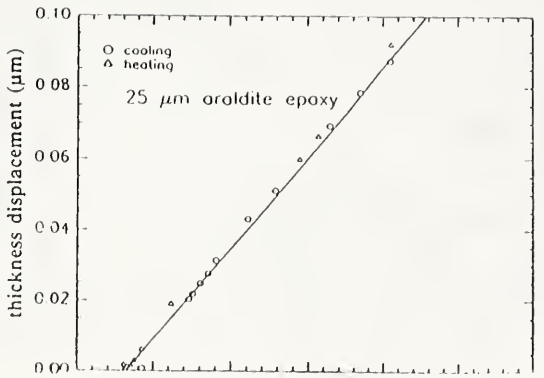
Thickness Direction Metrology

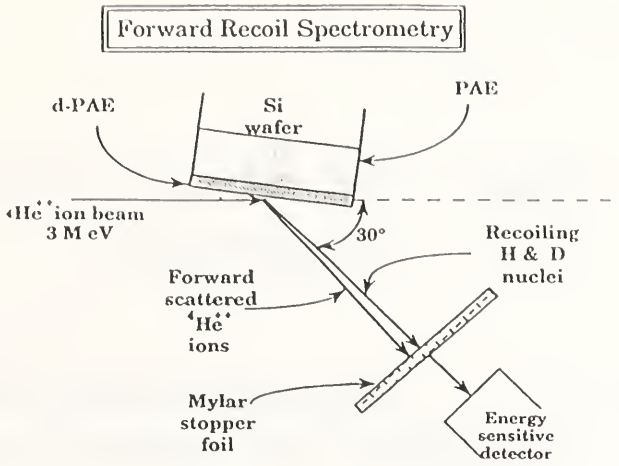
* Apparatus



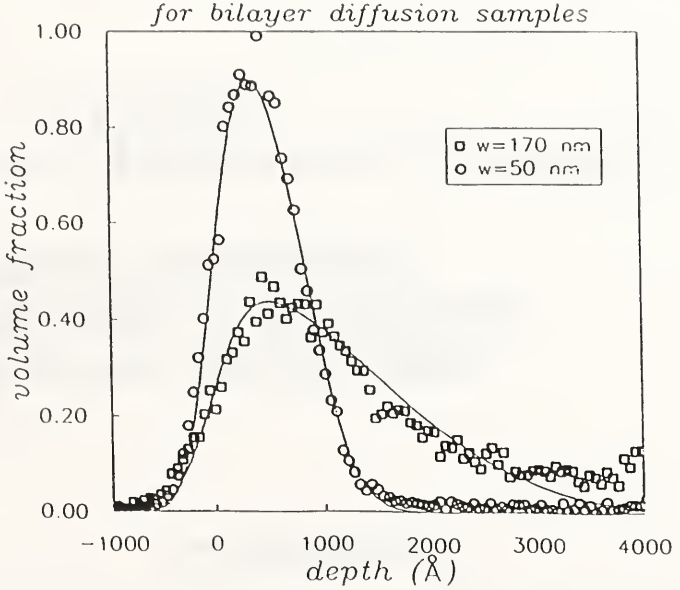
* Adhesive films processed in-situ. Free-standing films are constrained w adhesive.

* Data gives displacement vs. stress or temperature. Typical thermal data follows:



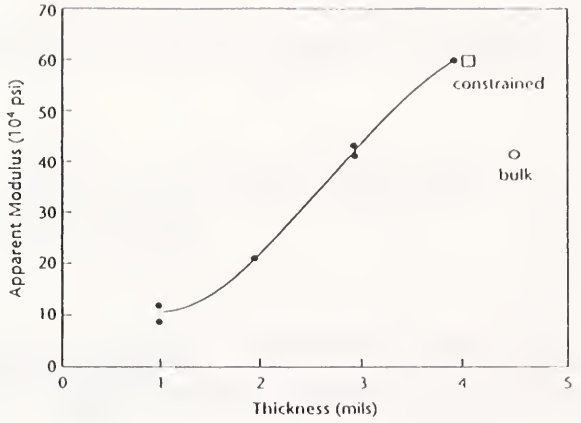


Deuterium depth profile obtained using FRES for bilayer diffusion samples

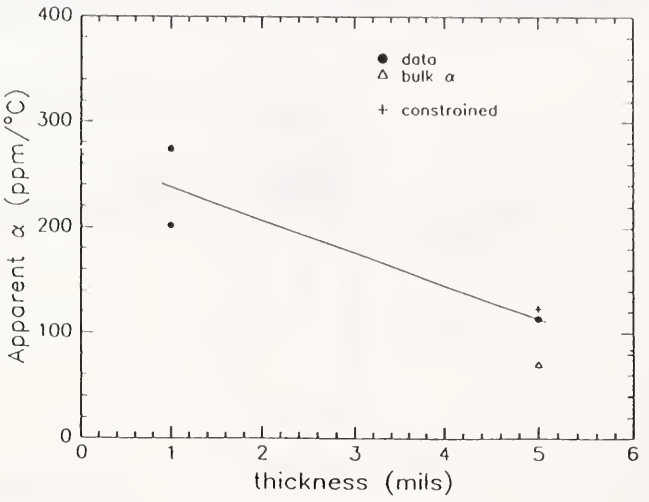


Results for an Epoxy Adhesive

* Elastic Modulus



* CTE



Constrained Deformation Equations
(transverse isotropy)

* Elastic modulus

$$\frac{1}{E_Z} = \frac{\Delta \epsilon_z}{\Delta \sigma_z} + \frac{2 (\nu_{xz})^2}{(1-\nu_{yx})\, E_x}$$

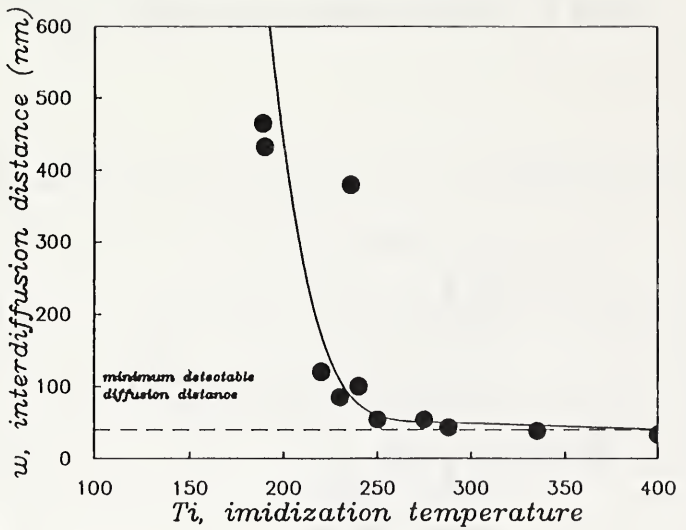
* CTE

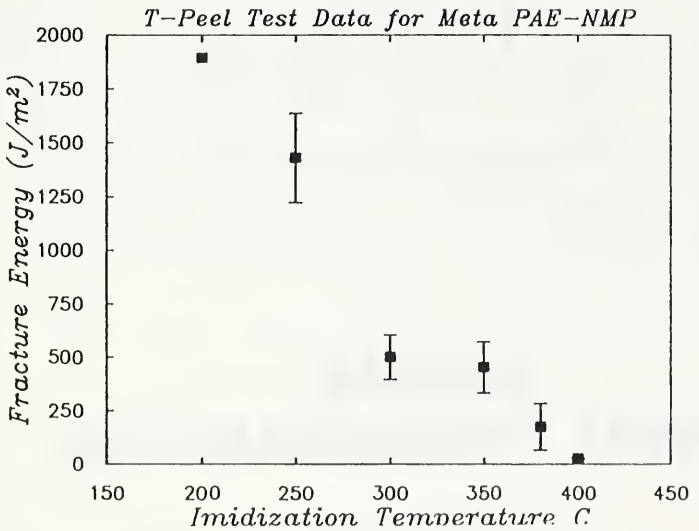
$$\alpha_Z = \frac{\Delta \epsilon_z}{\Delta T} - 2 (\alpha_x - \alpha_s)\, \nu_{xz} / (1-\nu_{yx})$$

* Poisson's ratio (rank one tensor):

$$\nu_{ij} = -\frac{\epsilon_{jj}}{\epsilon_{ii}}$$

=> Developing metrology for ν_{xz}





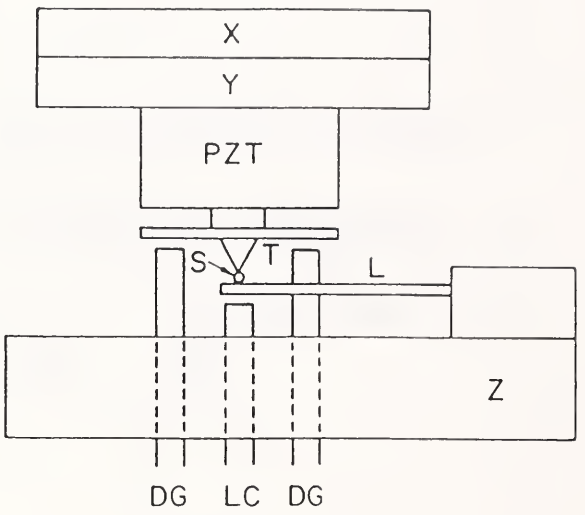
Microindentation Capabilities

1.	Load Resolution	< 2.5 μN
2.	Position Resolution	< 2.5 nm
3.	Temperature Stability	0.01 °C
4.	Vibration Level	< 1.0 nm

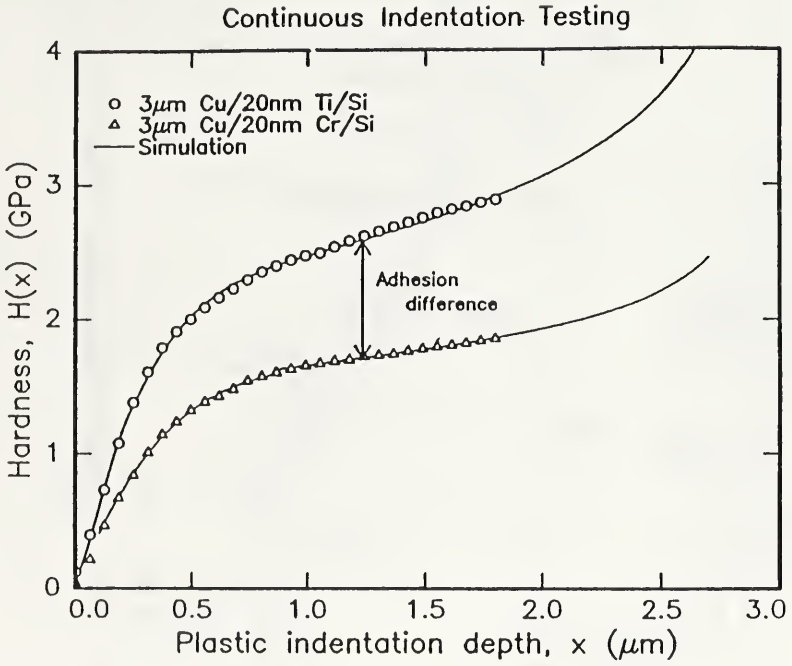
Advantages:

1. Probe small volumes.
2. Precise load and depth information.
3. Detection of small variations in deformation behavior.
4. Allows determination of Rate-Dependent Plasticity.

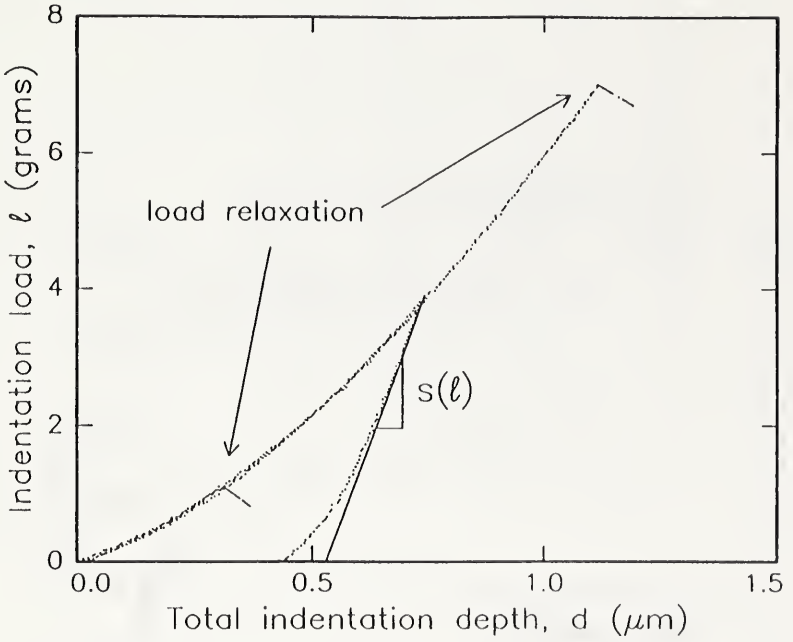
Microindentation Testing System



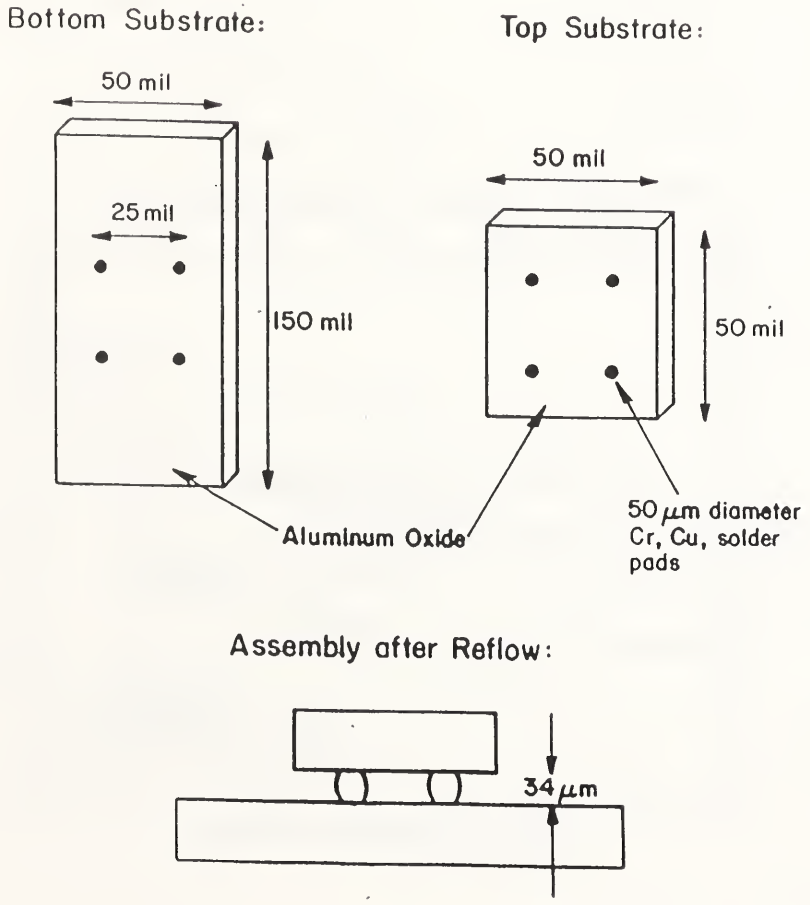
Effect of Interfacial Adhesion on Thin Film Hardness



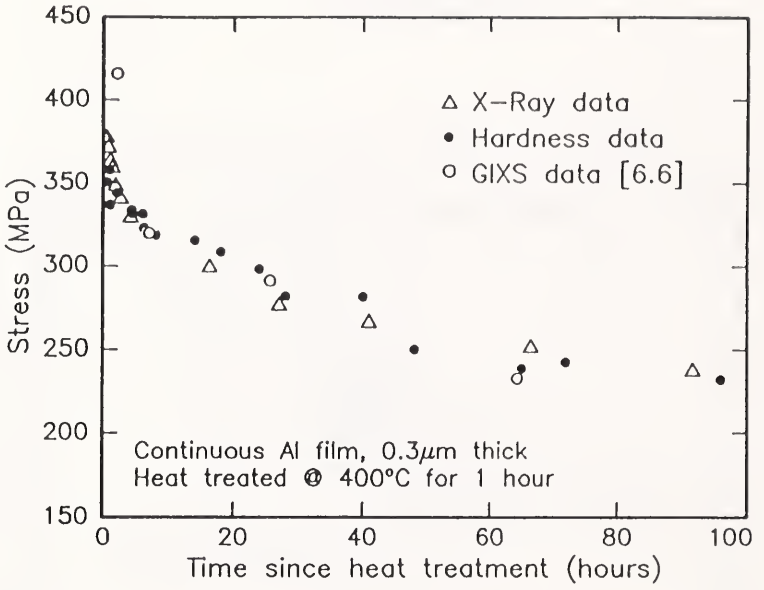
Typical Load-displacement Data of Microindentation Test



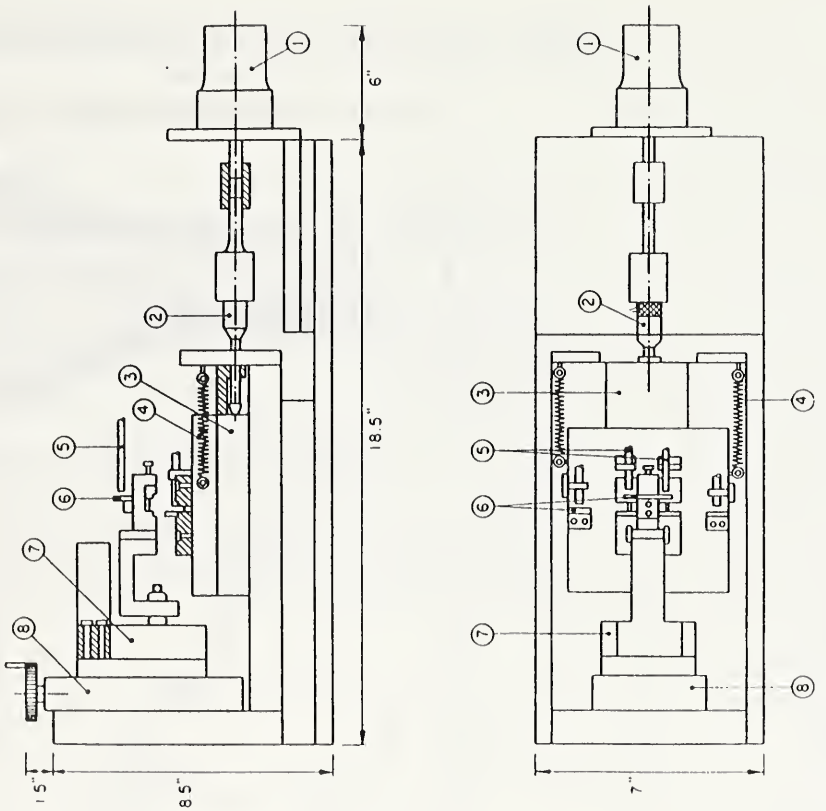
Test Sample Configuration



Relaxation of Residual Stress in Thin Films

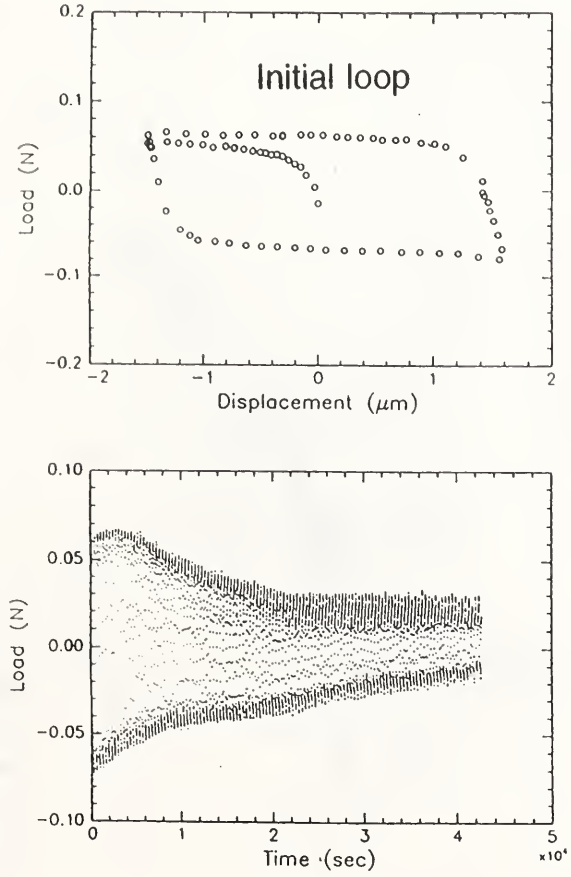


Microtensile Testing System



NO.	PARTICULARS
1	Motor
2	Micrometer
3	Horizontal Stage
4	Retaining Spring
5	Contactless Displacement Probe
6	Probe Target
7	Load Cell
8	Vertical Translation Stage

Isothermal shear testing of 2mil 97Pb/3Sn flip chip solder joints

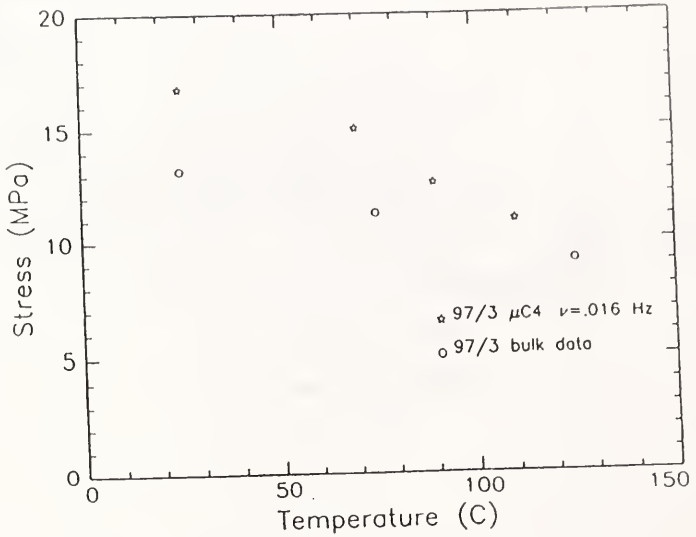


Flow Stress Vs. Temperature (97Pb/3Sn)

(☆) 2mil shear data, converted to uniaxial tension

(o) bulk data, uniaxial tension

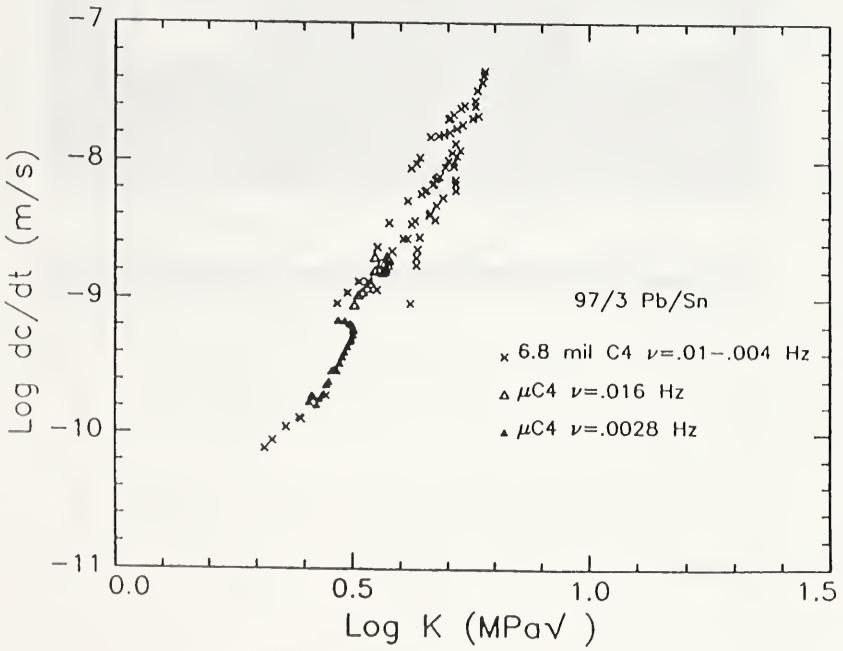
Hall-Petch effect!



Room Temperature Crack Growth Rate

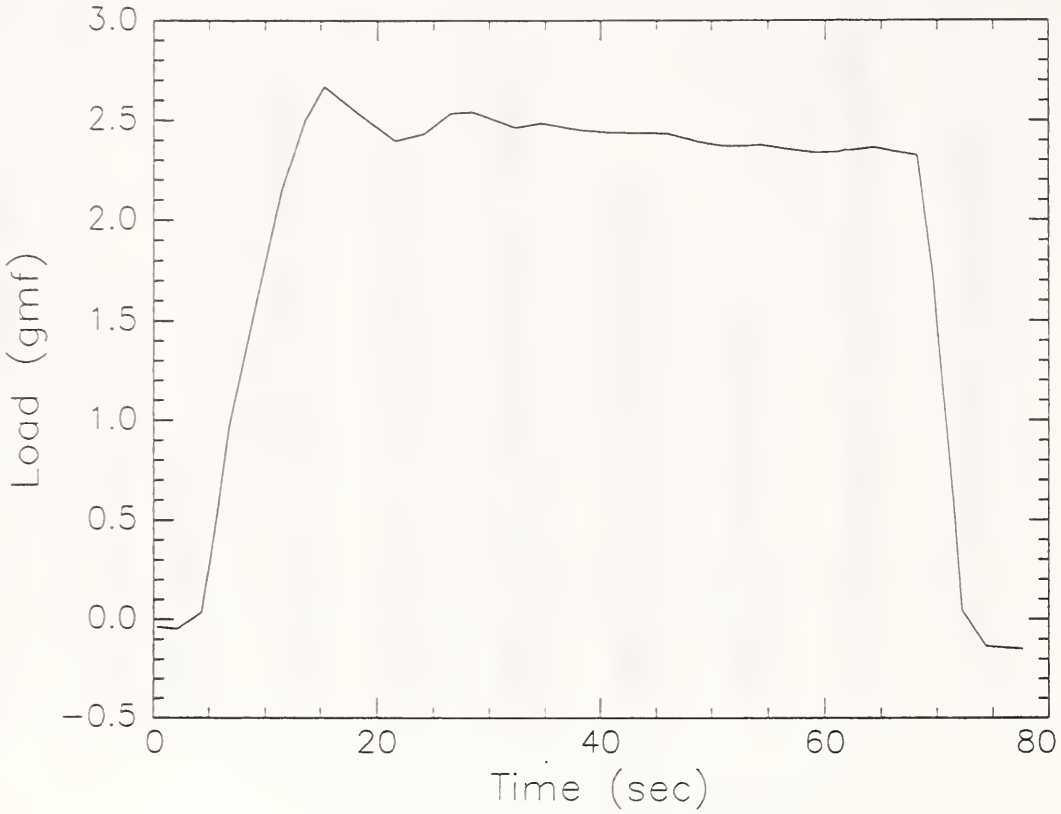
Dependence on initial solder joint size, L:

dc/dt scales with
'normalized stress intensity factor' $K=\sqrt{(L_o/L)}\,\sigma\sqrt{c}$
where L_o is 'unit length' (1m)



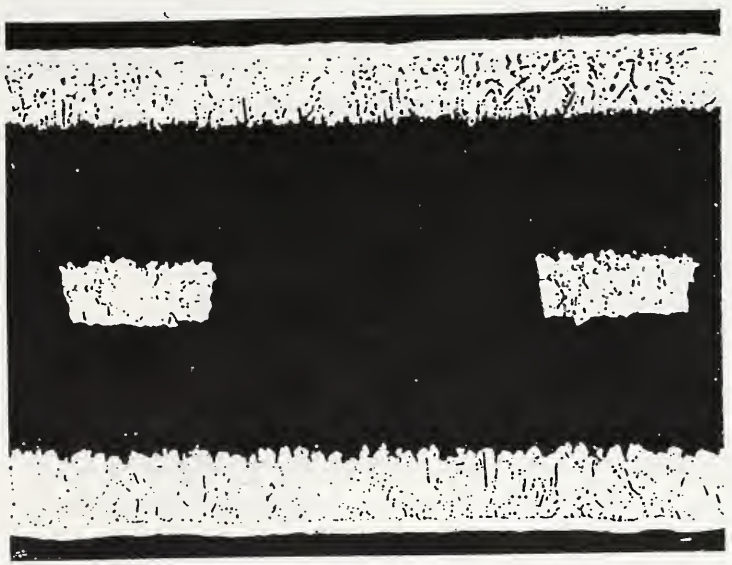
WAFER PROBE CONTACT RESISTANCE

* TOTAL SCRUB 10 μm OVER 30 SEC.
* PLATED NI BUMP CONTACTING PARTIALLY OXIDIZED 100% AL FILM
* BUMP REPLACES INDENTER ON MICROINDENTATION MACHINE. SCRUB PROVIDED BY MOTORIZED STAGE
* THE BUMP IS ~25 μm HIGH, ROUGHLY HEMISPHERICAL


3.0
2.5
2.0
1.5
1.0
0.5
0.0
−0.5
Load (gmf)
0
20
40
60
80
Time (sec)

20
15
10
5
0
Resistance (Ω)
scrub
0
20
40
60
80
Time (sec)

Cross-section of a High Performance Cable

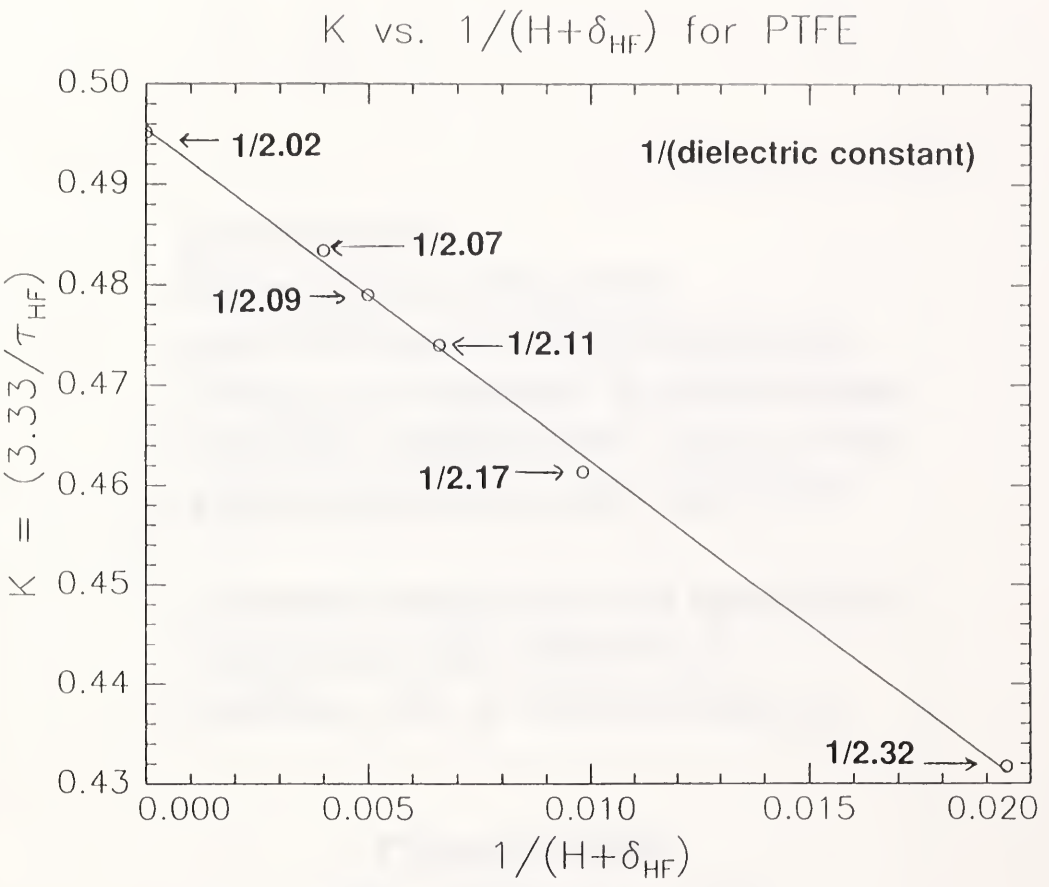


High Speed PCB Laminates

- Copper foil is chemically or mechanically treated to improve adhesion to dielectric
- This treatment may increase surface roughness, which will result in a slower propogation time constant and frequency dependent electrical properties.

Definitions for high speed PCB model

H = dielectric thickness
B = conductor stripe width
d_{EX} = external surface displacement (surface roughness)
δ = skin depth
C = $\varepsilon_r\varepsilon_0 B/(H-2d_{EX})$
L = $\mu_0(H+\delta)/B$
τ = $(LC)^{1/2}$ (propogation time constant)



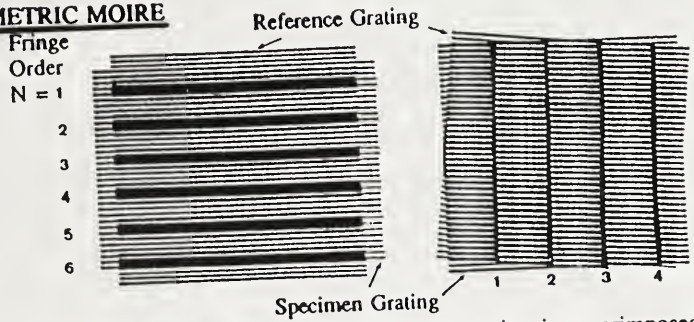
IBM MICROELECTRONICS

MOIRE INTERFEROMETR

ENDICOTT ELECTRONIC PACKAGING

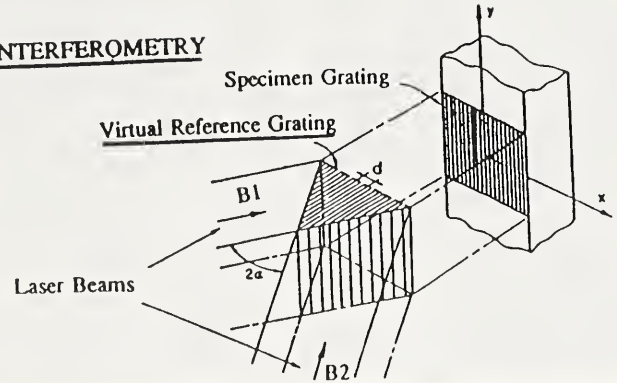
PRINCIPL

- **GEOMETRIC MOIRE**



Principle of the moire method: A reference grating is superimposed on a specimen grating and fringe patterns are formed by the interaction of the two gratings. The fringes, dark and bright bands, are contour lines of displacements. When the frequency of the reference grating is fixed, the fringes represent the specimen deformations.

- **MOIRE INTERFEROMETRY**



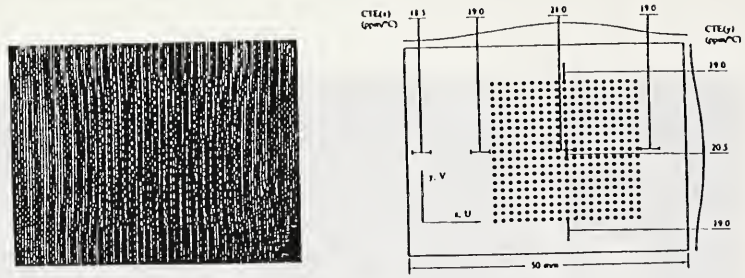


Fig. Effective CTE distribution of a FR-4 PCB.

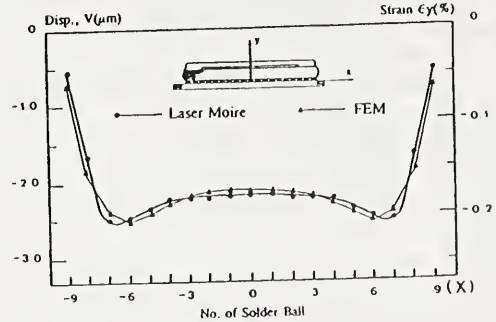
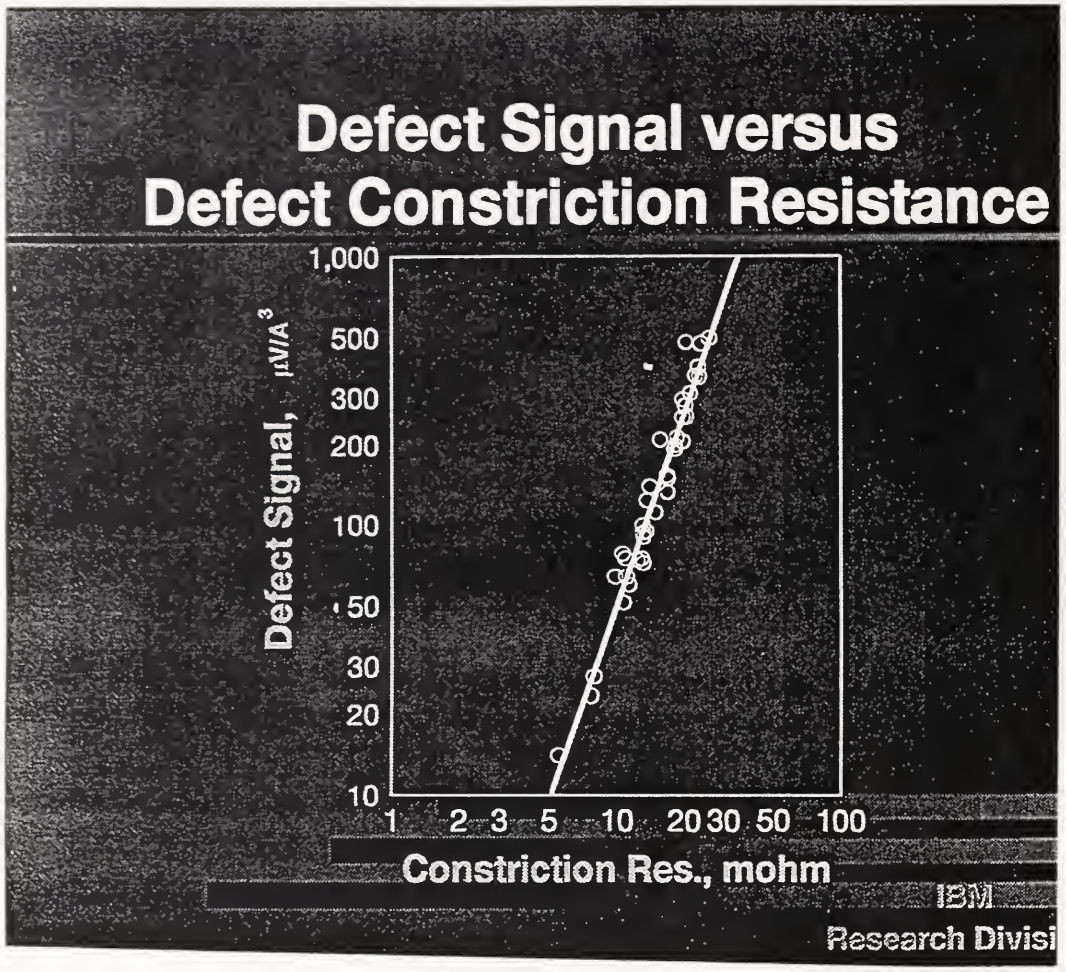
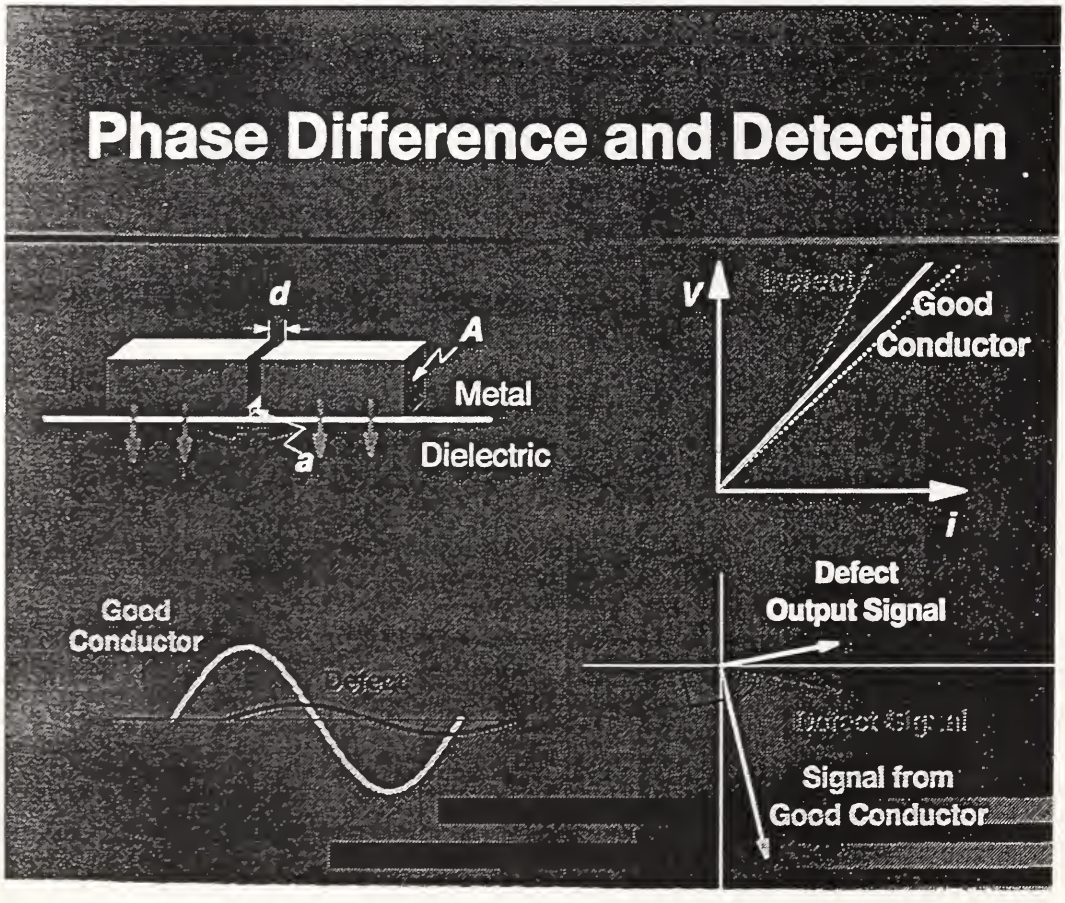


Fig. (a) V or vertical displacement field. (b) Comparison between experimental data and numerical prediction


Defect Signal versus
Defect Constriction Resistance
Defect Signal, μV/A³
1,000
500
300
200
100
50
30
20
10
1
2
3
5
10
20
30
50
100
Constriction Res., mohm
IBM
Research Divisi

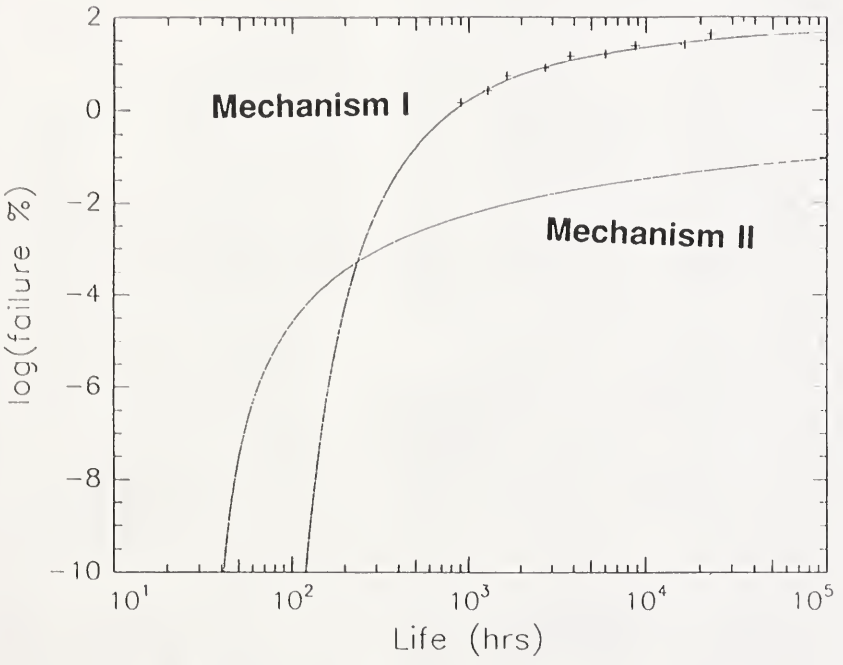

Phase Difference and Detection
d
A
Metal
Dielectric
a
V
Defect
Good
Conductor
i
Good
Conductor
Defect
Defect
Output Signal
Signal from
Good Conductor

Application Parameters

Item	Low frequency tester	High frequency tester
Detection frequency	2 KHz	455 KHz
Application	MCM - L	MCM - C, D, & L
Typical line thickness	15 - 75 μm	3 - 40 μm
Typical line width	50 - 250 μm	10 - 100 μm
Max. line resistance	5 ohms	20 ohms
Max. RMS current	520 mA	290 mA
Min. detectable defect resistance	0.003 ohms	0.010 ohms
Max. open circuit voltage	4.5 volts	0.2 volts

IBM
Research Division

Statistical Significance



Issues:

- Physically Based Model
- Experimental Accessibility

Weakest Link Rule

$$f(n) = 1 - [\,1 - f(1)\,]^n$$

$$f(n) = n\,f(1)$$

f(1): Life distribution of 1 segment
f(n): Life distribution of n independent segments

Conclusions and Challenges

- Advanced Measurement Techniques are available
- Statistical significance requires:
  - Physically based modelling
  - Experimental access

Conclusions and Challenges (continued)

- Statistically significant data from realistic specimens
- Physical models with optimum level of detail for data correlation and extrapolation

John Kelly, SRC

The workshop roadmaps address leading-edge, mainstream IC technology. Device technology needs for a broad range of memory and logic requirements drive the roadmap.

Workshop discussions focused on achieving key IC device characteristics as summarized in Table 1. Entries in this chart are organized by date of production start up; however, individual values reflect attributes of each technology generation at maturity. These characteristics were starting points for working group deliberations. The values are intended to focus attention on critical issues. The working group conclusions (for instance, in wafer processing cost) did not necessarily meet all the goals.

TABLE 1
OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

	1992	*1995*	*1998*	*2001*	*2004*	*2007*
Feature size (μm)	0.5	0.35	0.25	0.18	0.12	0.10
Gates/chip	300K	800K	2M	5M	10M	20M
Bits/chip						
– DRAM	16M	64M	256M	1G	4G	16G
– SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm^2)	$4.00	$3.90	$3.80	$3.70	$3.60	$3.50
Chip size (mm^2)						
– logic/μprocessor	250	400	600	800	1000	1250
– DRAM	132	200	320	500	700	1000
Wafer diameter (mm)	200	200	200–400	200–400	200–400	200–400
Defect density (defects/cm^2)	0.1	0.05	0.03	0.01	0.004	0.002
No. of interconnect levels — logic	3	4-5	5	5-6	6	6-7
Maximum power (W/die)						
– high performance	10	15	30	40	40–120	40–200
– portable	3	4	4	4	4	4
Power supply voltage (V)						
– desktop	5	3.3	2.2	2.2	1.5	1.5
– portable	3.3	2.2	2.2	1.5	1.5	1.5
No. of I/Os	500	750	1500	2000	3500	5000
Performance (MHz)						
– off chip	60	100	175	250	350	500
– on chip	120	200	350	500	700	1000

Typical characteristics of the range of product applications covered by this mainstream technology are shown in Table 2.

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS
DRAFT DATE 3/17/94

Year of first shipments	*1995*	*1998*	*2001*	*2004*	*2007*	*2010*	Notes (see Glossary)
Minimum feature (μm)	*0.35*	*0.25*	*0.18*	*0.12*	*0.10*	*0.08*	DRAM poly/contact
Memory (DRAM/Flash)							
- Bits/chip	64M	256M	1G	4G	16G	64G	
- cost/bit @volume (m¢)	0.1	0.05	0.02	0.01	0.005	0.002	[illegible] cut-down die
Logic (μProcessor, ASIC)							
- Gates/chip (cust. layout)	5M	10M	20M	50M	100M	200M	
- Cost/gate-MHz (m¢)	0.02	0.01	0.004	0.001	0.0004	0.0001	
- Gates/chip (auto layout)	800K	2M	5M	10M	20M	50M	
- NRE cost/gate (m¢)	5	2	0.5	0.2	0.05	0.002	
No. of chip I/Os							
- chip to test (pads)	•	•	•	•	•	•	• new number
- chip to package (pads)	750	1500	2000	3500	5000	7500	
No. of package pins/balls							
- μProcessor/controller	512	512	512	?	?	?	new assembly paradigm
- ASIC	750	1000	1200	1500	1800	2000	
Chip size (mm^2)							
- logic/μProcessor	260	400	640	700•	1000•	1400•	• multi-chip device
- DRAM	200	320	500	700	1000	1400	2 die per reticle??
Max no. wiring levels (logic)							
- on-chip	4-5	5	5-6	6	6-7	7	
- package plane	1	3	4	4	5	5	
Min mask count	18	20	20	22	22	24	
Cycle time (days theoretical)	8	8	8	9	9	9	
Max substrate diam. (mm)							
- Bulk or Epi wafer	200	200/300	300/400	300/400	400	400	*[illegible] uncertainty
- SOI wafer	200	200	200	300	300	300	[illegible] SOI viable
Max substrate diam. (mm)							
- MCM-D package plane	200	300	300	400	large rectangle	large rectangle	interposer/MCM-Si
Power supply voltage (V)							
- desktop	3.3	2.5	2.5?	1.5	1.5	0.9	
- battery	2.5	1.8-2.5	0.9-1.8	0.9	0.9	0.9	
Max power (W/cm^2)							
- high perf. wo/w heatsink	5/30	7/50	10/100	10/100	10/100	10/100	
- battery	4	4	4	4	4	4	
Test							
- cost/pin ($K)	6.7	3.3	2.5	1.4	1.0	0.7	
- No. of test vectors	8M	16M	16M	8M	4M	2M	
Design							
- % Normalized Cost	100	90	80	80	80	70	
- % BIST	30	50	70	90	90+	90+	

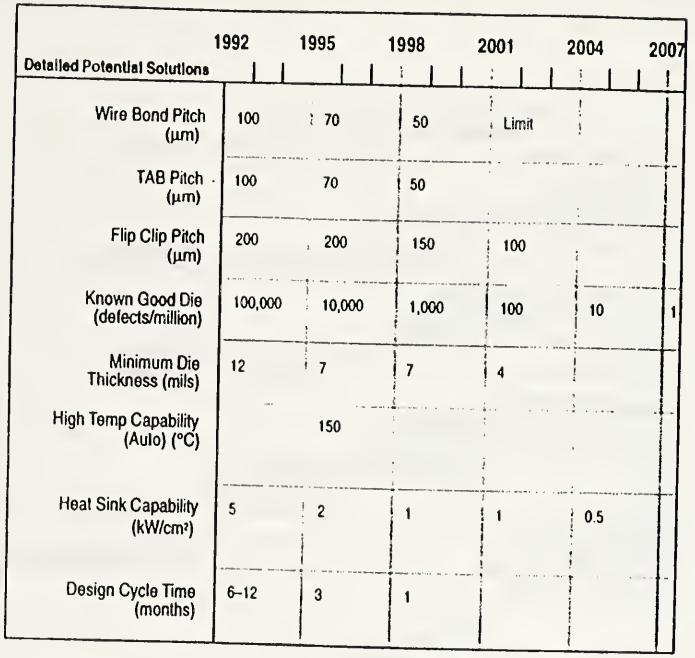


Figure 30 Packaging Needs

Packaging Core Competencies

- Electrical, Mechanical, and Thermal Design Modeling Simulator Capability
- Wave-Form Integrity Preserving Technology for Power/Ground and Signals (Interconnect and Substrates)
- Thermal Management and Thermal Mechanical Technologies
- Environmental Protection
- Cost Effective Quality Manufacturing (Test and Assembly — Largely Offshore)

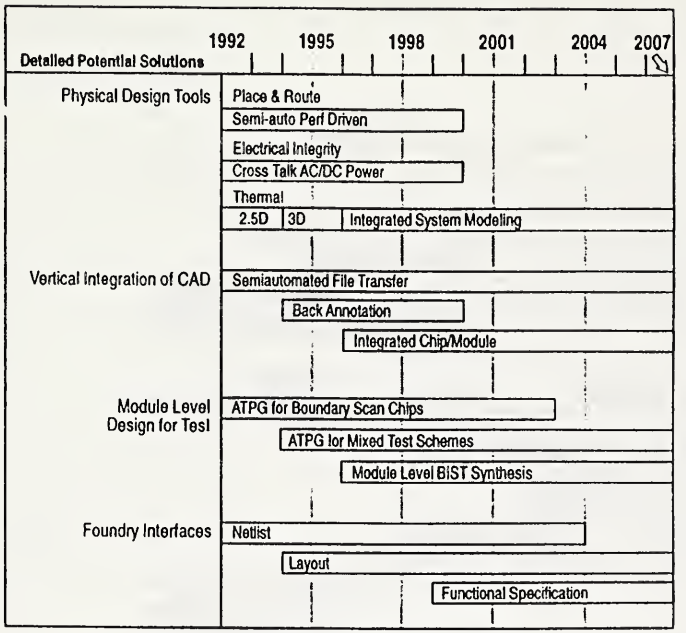


Figure 31 Packaging Roadmap: Module Design

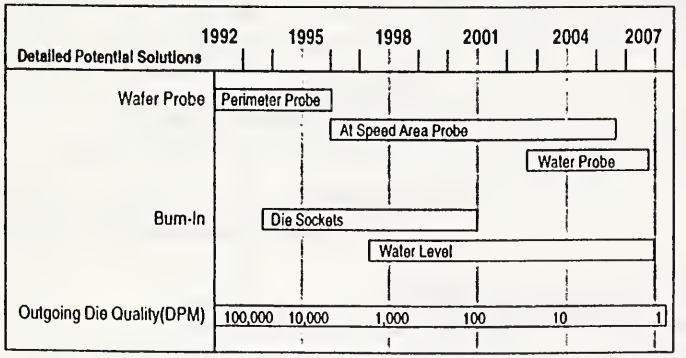


Figure 32 Packaging Roadmap: Known Good Die

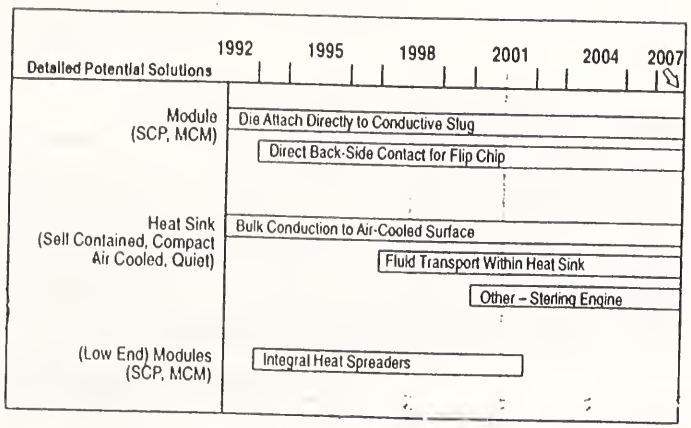


Figure 33 Packaging Roadmap: Thermal Management
(100,000 shipped)
(leading edge workstation)

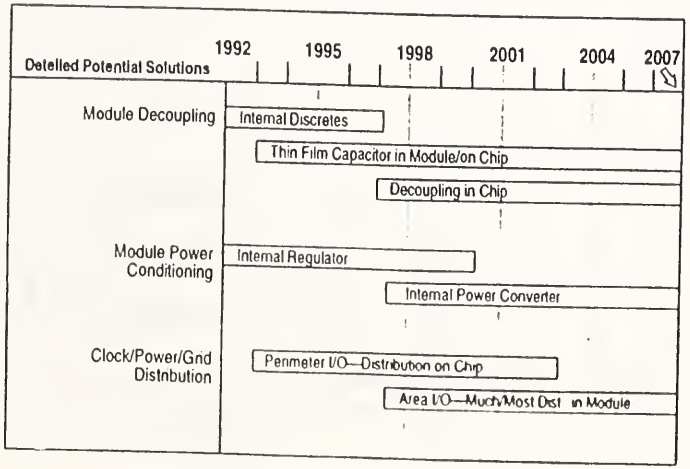


Figure 34 Packaging Roadmap Power Conditioning
(100,000 shipped)

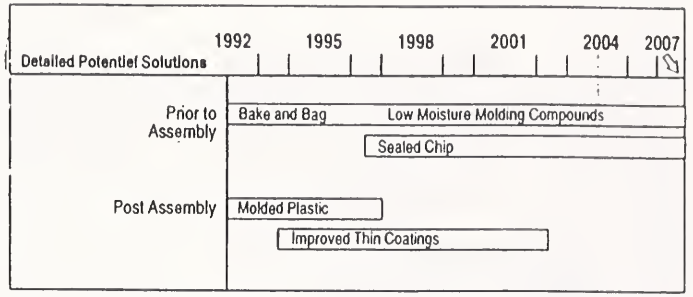


Figure 35 Packaging Roadmap: Environmental Protection
(100,000 shipped)
(Non-hermetic)

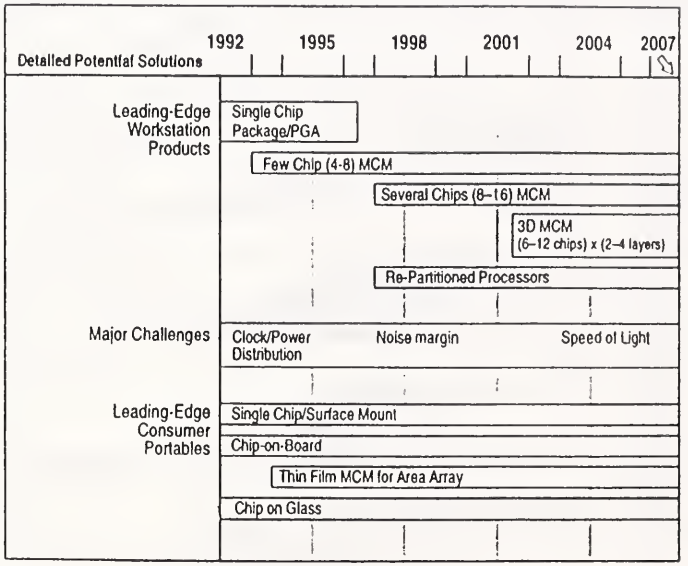


Figure 36 Packaging Roadmap: Product-Driven Demands
(100,000 shipped)

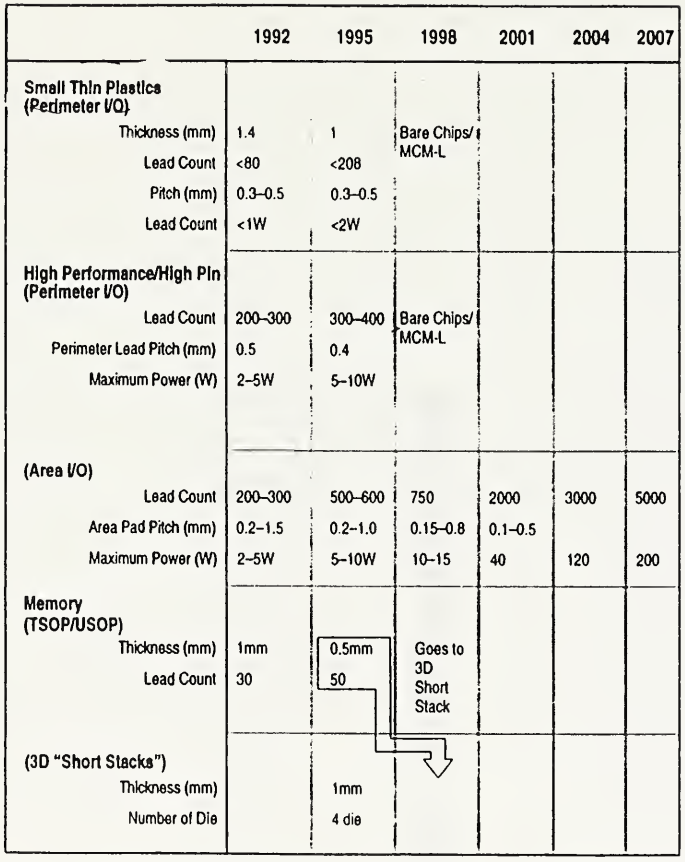


Figure 37 Packaging Roadmap: Highest Volume Products (>80% of development effort)

David Bergman, IPC

PROGRAMS

- SEMINARS
- STATISTICAL SERVICES
- MARKETING DATA
- STANDARDS/SPECIFICATIONS
- TECHNICAL REPORTS
- HOW'S BUSINESS SURVEYS
- TESTING PROGRAMS
- WORKSHOP/TRAINING
- PROFICIENCY CERTIFICATION
- RESEARCH

PROGRAM REQUIREMENTS

- CONSENSUS
- DIRECTION
- FOCUS
- SCHEDULING
- FLEXIBILITY
- VISION
- ORGANIZATIONAL STRUCTURE

IPC Present Status

680	Regular Members
570	Allied Members
415	Associate Members
115	Technical Liason Members
105	Government Members
1885	TOTAL

ELECTRONIC INTERCONNECTION INDUSTRY TECHNOLOGY ROADMAP

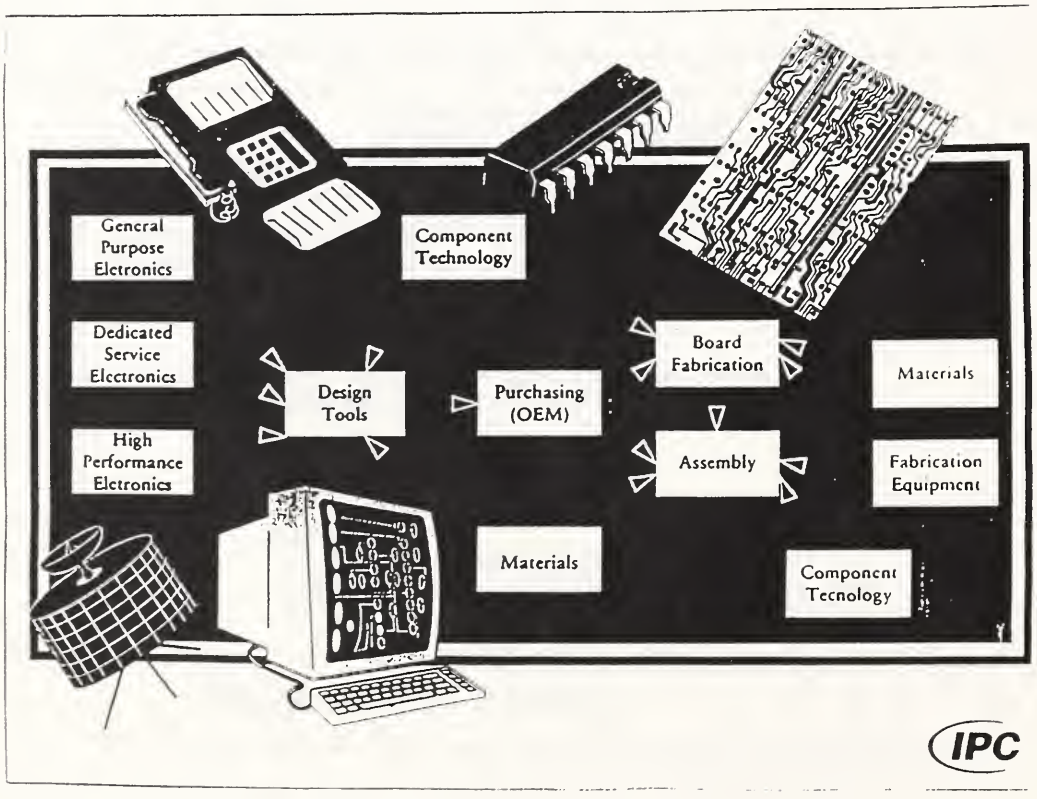
- MAP MAKERS
- DIRECTION
- DISTANCE
- FOCUS
- CHANGES
- RULES OF THE ROAD

TECHNOLOGY ROADMAP

INCLUDES ALL MEMBERS OF THE SUPPLY CHAIN FOR VIEWS ON COMPONENTS, OEM MANUFACTURING ISSUES, MATERIALS, INDUSTRY TOOLS AND MANUFACTURING SERVICES

METHODOLOGY BASED ON:

- COOPERATION
- COORDINATION
- COMMUNICATION



MEMBERSHIP SURVEY

C - COMPONENT PACKAGING
G - GENERAL ELECTRONICS
D - DEDICATED SERVICE
H - HIGH PERFORMANCE
T - DESIGN TOOLS
M - MATERIALS
F - FABRICATION
A - ASSEMBLY
P - PURCHASING

1993
1995
1997

THIS SURVEY WILL PROVIDE RESOURCE MATERIAL FOR DEVELOPING THE 1994 TECHNOLOGY ROADMAP OF SHORT TERM, AND LONG TERM REQUIREMENTS OF THE ELECTRONIC INTERCONNECTION AND ASSEMBLY INDUSTRY. YOUR PARTICIPATION IN THIS SURVEY IS PROBABLY **THE MOST IMPORTANT CONTRIBUTION THAT YOU MAKE FOR YOUR COMPANY AND THE INDUSTRY IN 1994.** IN ORDER TO COMPLETE THIS SURVEY, PLEASE ADDRESS ALL QUESTIONS IN WHICH YOU HAVE ANY INTEREST OR CAN PROVIDE AN INPUT.

PLEASE PROVIDE YOUR MOST IMAGINATIVE, INNOVATIVE, EVEN "BLUE-SKY" INPUT TO THE SURVEY.

WE WANT YOUR IDEAS FOR TODAY, TOMORROW AND BEYOND REGARDING THE NEEDS OF

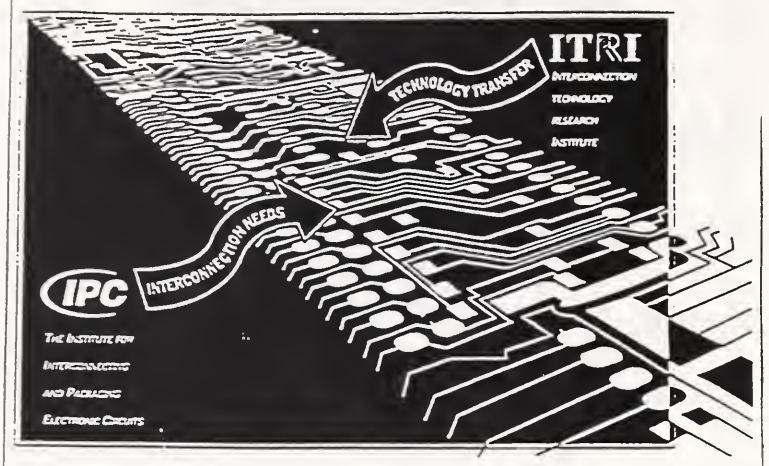
- THE ORIGINAL EQUIPMENT MANUFACTURER *that drives*
- THE ELECTRONIC INTERCONNECTION MANUFACTURERS *that drives*
- THE SUPPLIERS OF MATERIALS AND EQUIPMENT

SURVEY

FOR THE DEVELOPMENT OF THE 1994

ELECTRONIC INTERCONNECTION INDUSTRY TECHNOLOGY ROADMAP

PRELIMINARY SURVEY



TECHNOLOGY ROADMAP

THE FUTURE OF THE ELECTRONIC INTERCONNECTION INDUSTRY

MARCH 1994

RESPONDENTS

OVER 600
RECOMMENDATIONS FOR
1993 - 1995 - 1997

- TYPE OF RESPONDENT FUNCTIONS
  - MANAGEMENT
  - ENGINEERING
  - PRODUCTION
  - PURCHASING
  - QUALITY
  - PROCESS CONTROL
  - TECHNICAL LIAISON
  - VENDOR CONTROL
  - RESEARCH

SEVEN ISSUES PER TOPIC

FABRICATION EXAMPLE

F1 INNERLAYER LINE WIDTH AND SPACE
F2 BOARD SIZE
F3 BOARD & INNER CORE THICKNESS
F4 HOLE SIZES (THROUGH, BLIND, BURIED)
F5 NUMBER OF LAYERS
F6 TEST AND EVALUATION
F7 SURFACE CONDITIONS

THE MAP MAKERS

- TECHNOLOGY ROADMAP WORKSHOP

  - 100 EXPERTS MET IN APRIL
  - THREE DAY INTENSIVE REVIEW
  - TECHNOLOGISTS PRESENTATIONS
  - ANALYSIS OF SURVEY REPORT
  - DEVELOPED ROADMAP INITIAL DRAFT

DETAILS OF FIRST ROADMAP DRAFT

- ALL NINE TOPICS AND THEIR DETAILED BREAKDOWN WERE DEVELOPED BY THE FACILITATORS AND THEIR TEAM MEMBERS

  - DISCUSSION
  - OUTLOOK
  - SUCCESS FACTOR
  - SHOWSTOPPERS
  - RECOMMENDATIONS

MAJOR SHOW STOPPERS

- LIMITED METHODOLOGY TO DEVELOP AND INTEGRATE NEW TECHNOLOGY INTO MANUFACTURING
- NO SINGLE SET OF INDUSTRY/ GOVERNMENT/ ECONOMIC PROGRAMS FOR THE SUPPLY CHAIN
- DESIGN TOOLS ARE NOT COORDINATED WITH PRODUCTION PROCESSES
- LACK OF ENVIRONMENTALLY FRIENDLY MATERIALS AND MANUFACTURING PROCESSES
- POOR CUSTOMER/ MANUFACTURING/ SUPPLIER RELATIONSHIPS

REQUIREMENTS FOR GLOBAL COMPETITIVENESS

- STRONG ELECTRONICS INDUSTRY
- HEALTHY MEMBERS OF SUPPLY CHAIN
  - ELECTRONIC EQUIPMENT DRIVES
  - PRINTED BOARD ASSEMBLY DRIVES
  - PRINTED BOARD FABRICATION DRIVES
  - MATERIAL/ PROCESSING SUPPLIERS

INTERNATIONAL ELECTRONIC EQUIPMENT REQUIRES GREATER:

- MINIATURIZATION
- COST REDUCTION
- PERFORMANCE
- RELIABILITY
  (QUALITY IS EXPECTED)

MAIN CAUSES OF NEEDS TO CHANGE:

- STIFF AND GROWING COMPETITION (SUBSIDIZED BY LARGE COMPANIES)
- SHIFT IN RESPONSIBILITY FOR RESEARCH AND DEVELOPMENT
- GROWTH AND DEMAND FOR ELECTRONIC PRODUCT PERFORMANCE

PRIORITIZATION MEETING

- SPECIAL REVIEW OF COMMENTS
- ANALYSIS OF 164 RECOMMENDATIONS
- BREAKDOWN ACTION
  - RESEARCH
  - NATIONAL INITIATION
  - MARKETING
  - COMMITTEE PROJECTS

GROUPING OF RECOMMENDATIONS

- TECHNOLOGY ASSESSMENT METHODS
- DESIGN TOOLS COMPETENCE
- NEW MATERIALS THAT WITHSTAND STRESS
- IMPROVE QUALITY AND RELIABILITY METHODS
- NEW ATTACHMENT MATERIALS
- CUSTOMER ACCEPTANCE OF NEW IDEAS
- SIMPLIFIED, EFFICIENT MANUFACTURING PROCESSES
- NON VISUAL, NON DESTRUCTIVE INSPECTION METHODS
- ENVIRONMENTALLY FRIENDLY, SAFE MANUFACTURING

PWB FABRICATION SHOWSTOPPERS

- LAMINATE AND FOIL FINISH
- IMAGING TECHNOLOGY
- TESTING
- AVAILABILITY OF CAPITAL EQUIPMENT
- HANDLING OF MATERIALS IN THE PROCESS
- NUMBERS OF PROCESS STEPS
- ENVIRONMENTAL CONDITIONS
- VERTICAL PARTNERSHIPS
- PROCESS AVAILABILITY

WORKSHOP DELIBERATION REVIEW

- TEAM PROJECT DESCRIPTION RECOMMENDATION FINE TUNING
- ORGANIZE PROJECT DESCRIPTIONS INTO FOCUS GROUPS
  - MATERIALS
  - TOOLS
  - FABRICATION
  - ASSEMBLY
  - OTHER
- TEAM FORMATION
  - (WEDNESDAY GROUPING)
  - (NEW LIAISONS)
- PROJECT ASSIGNMENT
  - (MINIMUM - 6 PROJECT ANALYSIS WRITE-UPS PER TEAM)

IMPLEMENTATION WORKSHOP STRATEGY

- RESOURCE MATERIAL 1993
- SUMMARY OF 1994 SURVEY
- BREAK INTO REAFFIRMATION TEAMS
  - (2) DESIGN TOOLS
  - (2) MATERIALS
  - (3) FABRICATION
  - (2) ASSEMBLY
- GOAL
  - ANALYZE RESOURCE DATA AND 1994 SURVEY RESULTS AND REAFFIRM, UPDATE, ENHANCE RECOMMENDATIONS

ACHIEVING COMPETITIVE EXCELLENCE

CHANGE THE WAY WE:

- MANUFACTURE PRODUCTS
- INTERACT WITH THE ENVIRONMENT
- TRANSFER DATA
- SERVICE THE CUSTOMER
- DEVELOP NEW TECHNOLOGY
- PURCHASE PRODUCTS

RECOMMENDATIONS FOR ACTION

- METHODS FOR ESTABLISHING KNOWN GOOD DIE
- FLUXLESS SYSTEMS AND PROCESSES FOR ATTACHMENT
- CORRELATION OF NOBLE METAL EFFECT ON EMBRITTLEMENT AND SOLDERABILITY
- REDUCTION OF COMPONENT PACKAGING COSTS THROUGH THE USE OF BULK FEED MECHANISMS
- REPAIR METHODS FOR FINE PITCH COMPONENTS
- HIGH YIELD PRODUCTION EQUIPMENT FOR EASE OF HANDLING BARE CHIPS AND FLIP CHIP APPLICATIONS
- CONDUCTIVE ADHESIVES (PHOTOIMAGABLE)

WORKSHOP DELIVERABLES

- PRESENTATION OF SUGGESTED RESEARCH BY TEAM LEADERS
- INPUT FOR PUBLISHING EXECUTIVE OVERVIEW OF 1994 ROADMAP
- COMMITMENT/INTEREST LEVEL IN FORMATION OF COOPERATIVE RESEARCH TEAMS
- COMMITMENT TO PARTICIPATE IN ITRI
- PUBLICIZE INDUSTRY PROACTIVE POSITION

Rigid Printed Board Substrate Materials

- Develop core material less than 0.002 inch thick
- Develop clad laminate with smooth surfaces with fine conductors
- Form consortia to correlate UL 4-point oven aging with other methods
- Develop techniques to minimize environmental impact of producing base materials
- Develop materials which reduce hole formation costs
- Develop relationship between plated through-hole failure and measurable physical properties of rigid laminate

Conductors

- **Lack of characterization and measurement methods for thin foils, as well as lack of thin foil handling techniques are serious concerns**

Dielectric and Electrical Properties

- **Develop low Dielectric Constant (DK) substrates**

Component Attachment Materials

- No proven alloy alternatives for tin-lead solders
- Lead-free solders may be driven by environmental and political concerns rather than technical reasons
- Conductive adhesives have the following problems:
  - Moisture absorption which impacts adhesion
  - Poor mechanical shock properties
  - Poor high frequency (10mHz) performance
  - Undesirable high temperature properties

Board and Inner Board (Core) Thickness

- Establish techniques and equipment for handling thin materials

Surface Conditions/Coatings

- Eliminate metallic coatings by promoting use of bare copper with protective coatings and encourage R&D for compatible fluxes and reliable

Fine Pitch Technology

- Correlate effects of noble metals on surface quality, embrittlement and solderability

Attachment Techniques

- Develop fluxless systems and process
- Develop conductive adhesive applications and photo-imagable conductive adhesives

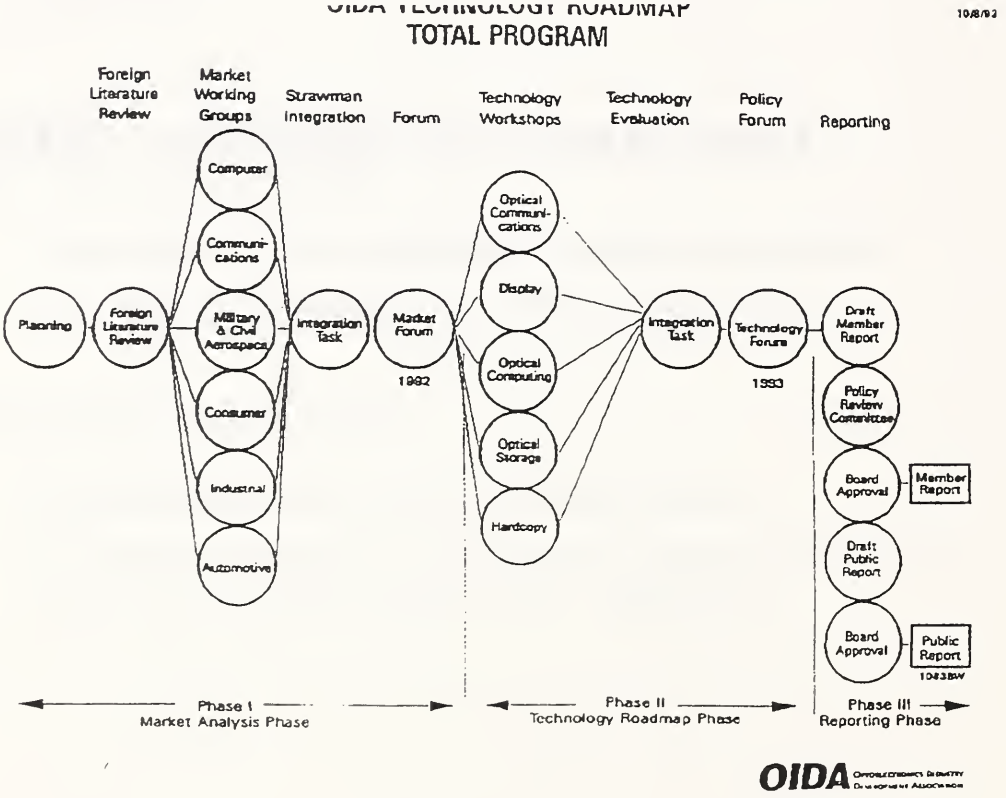
DAVIS HARTMAN, MOTOROLA, OIDA

OIDA TECHNOLOGY ROADMAP PROGRAM

DAVIS HARTMAN

MOTOROLA

OIDA



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OIDA TECHNOLOGY WORKSHOPS - PHASE II
ATTENDANCE SUMMARY

	Industry	Academic	Gov't	Total
Display	44	5	9	58
Optical Communications	55	5	4	64
Optical Storage	16	11	4	31
Optics in Switching & Computing	19	18	8	45
Hardcopy	26	3	1	30
	160	42	26	228

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OIDA TECHNOLOGY ROADMAP
BREAK-OUT DISCUSSION GROUPS

Display	Optical Communications	Optical Storage	Optics in Switching & Computing	Hardcopy
A. Passive Matrix LCD	A. Telecom	A. Media	A. Photonics in Switching	A. Printers - Electro-photographic
B. Active Matrix LCD	B. Datacom	B. Lasers and Optical Heads	B. Intramachine Interconnection	B. Printers - Inkjet
C. Electro-luminescent	C. Package Design and Mfg.	C. Noncon-ventional Optical Storage	C. Signal, Neural, Image, and Multidimensional Processing	C. Printers - Thermal/ Photo-sensitive
D. Plasma	D. Active Semiconductor Devices	D. Application-Driven Technology Requirements	D. Optical Memory Access and Data Base Systems	D. Media
E. Field Emission	E. Passive Devices			E. Scanners
F. LED	F. Fiber and Active Fiber Devices			F. Solid Imaging
G. 3D/Holography				
H. Projection				
I. CRT				

3624A

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Technical/Manufacturing Barriers for Flat Panel Displays

- PMLCD
  - Limited contrast, color saturation, response time, resolution
- AMLCD
  - Complex, high-cost processing
- Electroluminescent
  - Poor gray scale capability, high cost ICs, limited color
- Plasma
  - Poor gray scale, low luminous efficiency, high-cost ICs
- Field emission
  - Difficult spacer fabrcation and vacuum assembly; needs development of cathode technology

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DISPLAY TECHNOLOGY ROADMAP

Field Emission

	1993	1998	2003	2008	2013
PARAMETER					
Screen resolution	240x320	1280x1024	1280x1024	HDTV	HDTV
Screen diagonal, inches (production, max.)	--	10	20	40	70
Pixel resolution, lines per inch	80	170	240	240	240
Duty ratio	240	1024	1024	1100	1100
White luminance, cd/m2	50	150	250	500	500
Contrast ratio @ ambient illum.	5	10	15	20	20
Gray levels @ CR	32	64	64	128	256
Number of colors	8	262K	262K	4M	16M
Viewing angle, +/- degrees					
Horizontal @ CR > 10:1	80	80	80	80	80
Vertical @ CR > 10:1	80	80	80	80	80
Panel response time, msec	< 16	< 16	< 16	< 16	< 16
Number of panel defects (10-in. color)	0	0	0	0	0
Total panel power, watts	5	2	10	100	200
Price, $	--	400	300	300	500
TECHNOLOGY DEVELOPMENTS					
Cathode manufacturing	--	10 inches	20 inches	40 inches	70 inches
Spacers	200 V	500 V	2,000 V	2,000 V	2,000 V
Low voltage phosphors	1 lumen/watt	5 lumens/watt	10 lumens/watt	12 lumens/watt	14 lumens/watt
Vacuum integrity/operating life	10,000 hours	20,000 hours	40,000 hours	60,000 hours	80,000 hours
Cost-effective computer screens	--	1024x1280	2048x2560		
Cost-effective video			HDTV	HDTV	
			30-40 inches	40-50 inches	

Recommendations for Flat Panel Display

- PMLCD
  - Further development of active addressing technology
- AMLCD
  - Development of low-temperature polysilicon process
- Electroluminescent
  - Develop a blue phosphor that does not require high temperature substrates
- Plasma
  - Develop phosphors with high luminous efficiency
- Field emission
  - Develop cathode plates, long-lived low-voltage phosphors, spacers

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Technical/Manufacturing Barriers for Optical Communications

- Cost of packaging and alignment of active and passive components
- Cost of fiber management
- Overconstrained requirements on device/package design
- Modeling/simulation/CAD tools
- Common approaches/standards in several areas, e.g. high-speed datacom
- Concurrent engineering (interaction between device and package design)

OIDA

TELECOMMUNICATIONS TECHNOLOGY ROADMAP

Local Loop/CATV Alternatives/Fiber to the Curb

		1993	1998	2003	2008	2013
GENERAL	Unit Cost ($/Home)	160	75	40	25	15
	Fiber	SM Glass	SM Glass	SM Glass	SM Glass	SM Glass
	Reliability, FITS		100	50	25	12.5
	Service – Migration to ATM					
	Low-Cost Fiber Management					
PASSIVE OPTICAL NETWORK (PON)	Line Rate, Mb/s	20	155	155	622	622
	Subscriber End Duplex Transceiver Cost, $	400	100	50	20	10
	Splitters: Type	Glass Fused	Glass Fused	Polymer	Polymer	Polymer
	Cost, $	40	29	10	5	3
SUBCARRIER MULTIPLEX (AM-VSB)	6 MHz Channels/Wavelength	80	160	320	640	640
	Wavelengths per fiber	1	4	4	8	16
	Modulation	Direct	Direct or External	Direct or External	Direct or External	Direct or External
	Wavelength	1300 nm	1300, 1550 nm	1300, 1550 nm	1300, 1550 nm	1300, 1550 nm
	Repeaterless Span, km	15	15	15	15	15
	Amplifiers					
	Wavelength Routing					
DIGITAL POINT-TO-POINT	SONET Line Rate, Mb/s	155	622	622	622	
	Bidirectional Link Component Cost, $	250	200	150	100	
	Transceiver Cost, $	75	38	19	9	
	Transmitter/Receiver Packages			Uncooled/Low-Cost Connectors		
	Lower Cost Fiber Management and Connection					

Recommendations for Optical Communications

- Transmitters and receivers
  - New packaging approaches with lower cost materials; automated alignment; high-yield processes for device fab
- Connectors
  - New low-cost materials, e.g. polymers and polymer/ceramic composites; less labor-intensive field installation methods
- Fiber/cable management
  - Improved design for fiber cable and fiber and cable management apparatus; new materials and tools
- Couplers, splitters and WDMs
  - Low-cost packaging and alignment approaches; elimination of pigtailing

OIDA Optoelectronics Industry Development Association

Technical/Manufacturing Barriers for Optical Storage

- Testing and measurement capability for magneto-optic media at high storage densities
- Molding and mastering of high-capacity substrates
- Low jitter noise media for pulse-width modulation
- Short wavelength lasers
- Integration of optical heads

OIDA Optoelectronics Industry Development Association

OPTICAL STORAGE TECHNOLOGY ROADMAP

PARAMETER	1993	1998	2003	2008	2013
Capacity, Gbit/sq. in.	0.5	4	32	>100	
Data Rate, Mbyte/sec.	1-2	6-9	>30	>100	
Access Time, msec	30-60	20-30	<10	<1	
Wavelength, nm					
Laser diode	780	680 (620)	480	400	
Frequency doubled		430-500	430-500	340-430	
Number of Beams	1	1-3	3-9	Beam deflection	
Price					
Drive, $ (130 mm)	1500	500	200		
Media, $/MB (130 mm)	0.1	0.01	0.005		
TECHNOLOGY DEVELOPMENTS					
Storage Technology	Magneto-optic	Magneto-optic	Magneto-optic	Holographic	
Media					
Materials	TbFeCo	Improved TbFeCo, phase change	High Kerr media	Photorefractive materials	
Form factor, mm	90, 130	62, 90, 130	46, 62, 90		
Recording					
Coding	Banded PPM	PWM	PWM, advanced codes		
Overwrite	Erase first	Direct			
Read/Write Head					
Integration	Discrete comps.	Partial integration	Full integration	Non-mechanical	
Form factor, mm		20x20x5	20x20x3		
Laser Diode Materials	AlGaAs	AlInGaP (CdZnSe)	ZnS	ZnSSe	

Recommendations for Optical Storage

- Short wavelength sources
  - Central facility for advanced engineering samples; address manufacturing scale-up issues
- Advanced media
  - Test center for evaluation of media under realistic conditions; new plastic substrate technology
- Advanced optial storage systems
  - Support for interdiscplinary programs involving applications/software/technology
- 3-D optical memories
  - Accelerate development of prototype recording systems; support 3-D materials R&D

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Technical/Manufacturing Barriers for Hardcopy Technologies

- Simplified, single-pass process for color electrophotography
- Low-cost high-power laser diodes, more sensitive media for thermal printing
- Post-exposure processing for photosensitive media
- Common color standards for scanning and reproduction
- Lower cost UV sources, improved photopolymers for solid imaging

OIDA

HARDCOPY TECHNOLOGY ROADMAP

Thermal/Photosensitive

PARAMETER	1993	1998	2003	2008	2013
Image quality, dpi	300/300	600/600	600/800	600/1000	600/1200
Line pair resolution, lp/mm	8/8	12/12	12/16	12/20	12/24
Dmax (reflective)	2.6/2.8	2.8/2.8	2.8/3.0	3.0/3.0	3.0/3.0
Dmax (transmissive)	2.2/3.5	2.5/3.5	2.8/3.5	2.8/3.7	2.8/3.7
Dmin (reflective)	0.03/0.06	0.02/0.05	0.02/0.04	0.02/0.03	0.02/0.02
Dmin (transmissive)	0.01/0.06	0.01/0.04	0.01/0.03	0.01/0.02	0.01/0.02
Halftone/gray scale levels	Continuous tone/8-12 bit x 3	———	———	———	——>
Speed (thermal 8x10)					
Time to first print, min.	5-10	1	0.5	0.25	0.25
Throughput, min. per print	2-5	<1	<0.5	0.1	0.1
Initial Cost, $000 (8x10)	8-10/60	2/30	1/10	0.5/5	0.2/3
Cost per page, ¢ (8x10)	2.50/1.40	0.80/0.70	0.70/0.50	0.70/0.50	0.50/0.40
Size	Desktop	Desktop	Portable	Smaller	Small
Dot Addressability, +/- micron	40/40	20/20	20/15	20/12	20/10
TECHNOLOGY DEVELOPMENTS					
Low-cost thermal printer		Better low-cost resistive head			
		Low-cost RIP			
High quality thermal printer			High-power, low-cost laser		
Laser diode cost, $/watt			100	50	25
New media	100x greater sensitivity				
Silver halide printer		Blue-green laser diode			
		Low-cost deformable mirror/LCD shutter			

Recommendations for Hardcopy Technology

- Solid imaging
  - Low-cost imaging system, including high-power UV laser and precision x-y scanning; photopolymers for engineering plastics
- Color standards
  - Research to determine a single, optimal color standard for all printing/scanning applications
- Software
  - Development of software to enhance the ease of use of color, i.e. automatic color rendering

OIDA

Lance Glasser, ARPA

Administration Initiatives in Electronics

industry
make profit,
satisfy customers

academia
educate students,
create knowledge

government
serve public good

The Electronics Subcommittee

ESC

Why the Federal Government is concerned with Electronics

- Competitiveness in electronics manufacturing is critical to the Nation
- There are major competitiveness issues facing the U.S. Electronics industry
- Government must work with the private sector to facilitate long-term U.S. leadership and economic competitiveness in Electronics

ref: AEA

The right people; the right time; the right focus

ESC

The Clinton Administration has established an Electronics Subcommittee (ESC) to help set priorities and coordinate Agency activities, comprising:

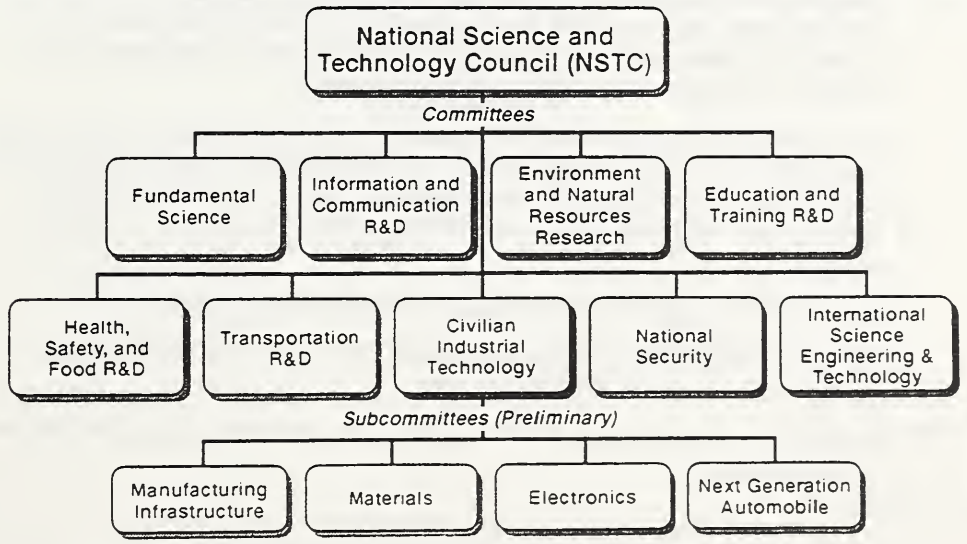
Office of Science and Technology Policy
National Economic Council
Department of Commerce
  National Institute of Standards and Technology
Department of Defense
Department of Energy
Environmental Protection Agency
National Aeronautics and Space Administration
National Science Foundation
National Security Agency
Critical Technologies Institute of RAND—Non-voting participant

rev 5/2/94, compact

The right people; the right time; the right focus

ESC

Organization of the National Science and Technology Council



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The right people; the right time; the right focus

ESC Electronics Subcommittee Mission

Provides interagency coordination for technical planning, budgeting, reporting, and evaluation of Federal programs in electronics science and technology and supports two-way communication on these programs within the government and with the private sector.

ESC Functions

- Reports to the Civilian Industrial Technology Committee (CIT) of the National Science and Technology Council (NSTC) and represents the advocacy position for electronics issues with all Federal interagency crosscuts or initiatives.
- Provides coordination of interagency technical program planning, budgeting, and reporting, and coordination with the private sector, in order to encourage the development and execution of joint government-private sector electronics R&D programs in priority areas.
- Provides a forum for government-private sector interaction
- Collects, maintains, and disseminates an up-to-date inventory of Federal electronics R&D programs.
- Proposes and develops joint government/private sector initiatives in electronics.

ESC

ESC activities and goals

Forums for government-private sector interaction

Focused initiative development (NEMI)

- Improve U.S. competitiveness and job creation in electronics and downstream industries

Inventory project

- Widely disseminate information on Federal government agency activities, priorities, strategic plans, and internal processes.
- Collect and maintain accessible data on electronics-related research and development activities in Federal agencies

Benchmarking activities

- Identify and measure key electronics competitiveness parameters

The right people; the right time; the right focus

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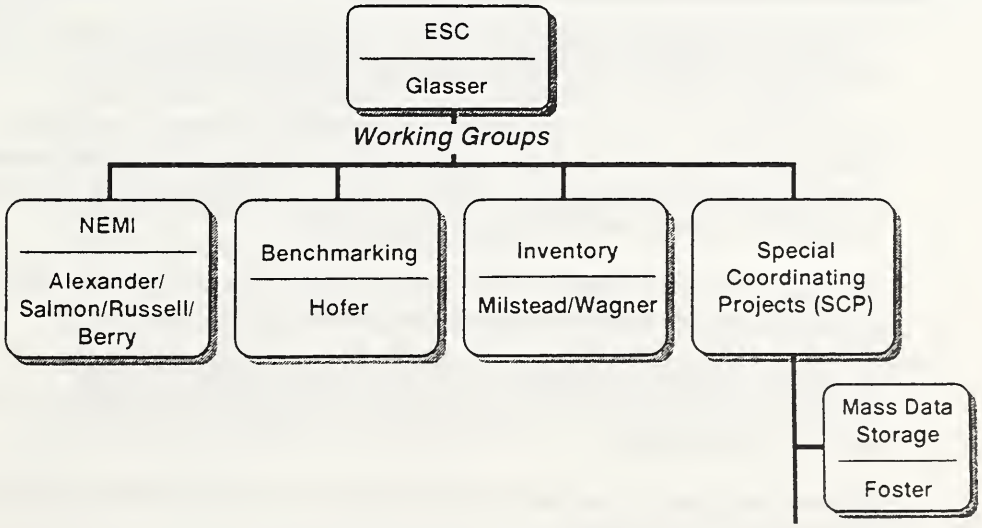
ESC

Electronics Subcommittee Organization



The right people; the right time; the right focus

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ESC

CTI inventory work with the Federal R&D Database

Tie four Major Government-wide Databases together. . .

MAX Budget Preparation System
Catalog of Federal Domestic Assistance
Federal Assistance Awards Data System
Federal Procurement Data System

OMB GSA DOC GSA

Augment with internal agency data collections:

DoD (R-1 w/ Descriptive Summaries, DROLS), HHS (CRISP), NASA (507 System), DOE (PADS), NSF (Mainframe), EPA (Awards System), DOD (Internal Files), USDA (CRIS), etc.

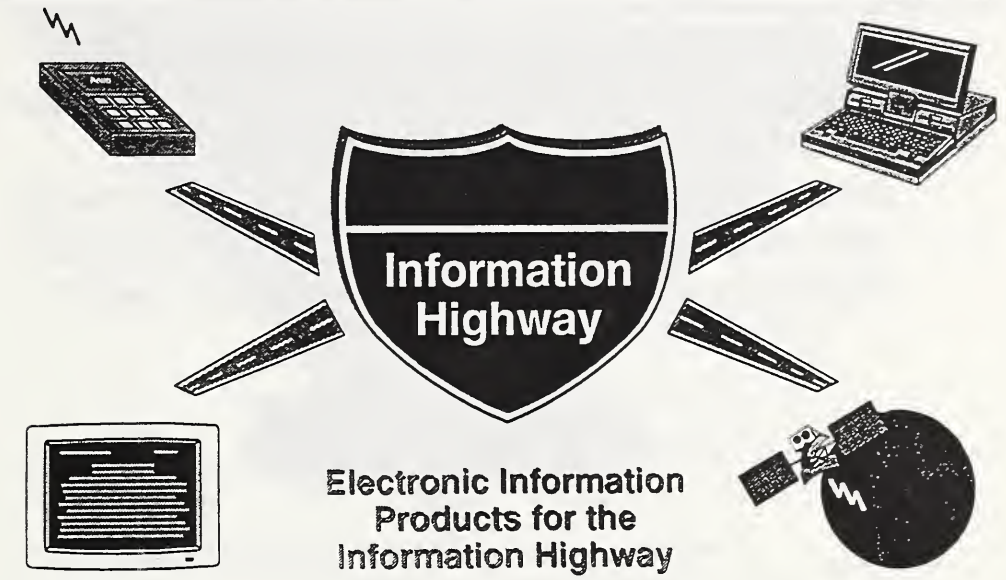
ESC

The concept of an abstract product focus

- The electronics industry is too broad and diverse to be encompassed by a single strategic plan or vision
- By picking a class of products on which to focus, one can develop a workable plan for infrastructure, policy, and research that supports the product class, with priorities and action items for government and the private sector
- The government does not actually build the products, which are only an abstraction used for planning purposes
- Industry builds products, with their own funds, on the infrastructure developed and within the policy envelope of the planned initiative
- Moreover, the initiative is expected to have benefit beyond the selected focus area

ESC

The National Electronics Manufacturing Initiative (NEMI)



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We have a vision for a focused Electronics Manufacturing Initiative

- Focus on electronic information products for the information highway—the National Electronics Manufacturing Initiative (NEMI).
- Government would provide support for enabling technology and infrastructure.
- Can deploy some existing government resources in FY94/95 (such as ATP or TRP) if the industry becomes enthusiastic and if a good plan is developed. On track to impact FY96 budget cycle.

The right people; the right time; the right focus

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National Motivation

Led by Vice President Gore, the United States is embarking on an aggressive program to network the nation with 21st-century information "superhighways." What hardware and software will connect to these information highways and which nation will make them?

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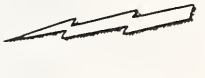
Attributes of Electronic Information Products that will drive technology decisions over the next decade

Delivers multiple information services to people

User interface centered

Connected to international-scale information infrastructures



Green life cycle

Low cost, highly reliable

Ubiquitous, huge but differentiated markets

Often mobile, portable, lightweight

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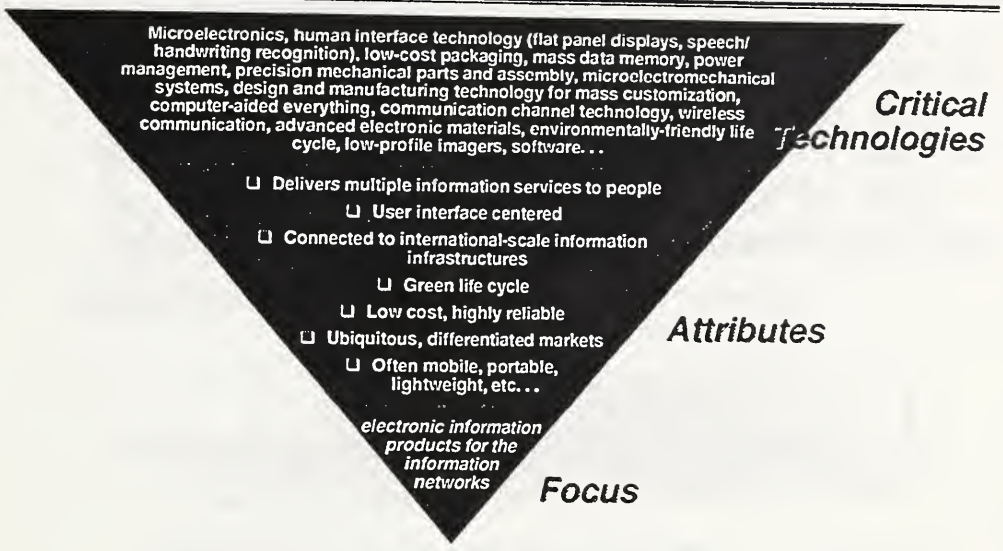
Focusing on make-a-difference R&D investments


Microelectronics, human interface technology (flat panel displays, speech/ handwriting recognition), low-cost packaging, mass data memory, power management, precision mechanical parts and assembly, microelectromechanical systems, design and manufacturing technology for mass customization, computer-aided everything, communication channel technology, wireless communication, advanced electronic materials, environmentally-friendly life cycle, low-profile imagers, software...
Critical Technologies
❑ Delivers multiple information services to people
❑ User interface centered
❑ Connected to international-scale information infrastructures
❑ Green life cycle
❑ Low cost, highly reliable
❑ Ubiquitous, differentiated markets
❑ Often mobile, portable, lightweight, etc...
Attributes
electronic information products for the information networks
Focus

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Policy issues will be overseen by the National Economic Council and the Office of Science & Technology Policy, e.g.,

- USG procurement
- Environmental regulation
- International technology transfer
  - Technology-for-technology initiative
  - U.S.-Japan technology framework negotiations
- Federal-States cooperative efforts
- Trade
  - Export promotion
  - Export control
- Facilitating Standards
- Labor issues specific to high-tech manufacturing
- SBIR increase and its relationship to Administration initiatives
- Intellectual property issues
- Infrastructure, such as NII or manufacturing extension services

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Government as consumer can accelerate development

Examples where the Federal government could be an early customer:

- Very low cost electronic tutors/assistants for accelerating education and training
- Distributed environmental sensor networks
- Systems of sensors and actuators for Federal building energy savings
- Smart National health cards
- Hand-held Military Information Associates

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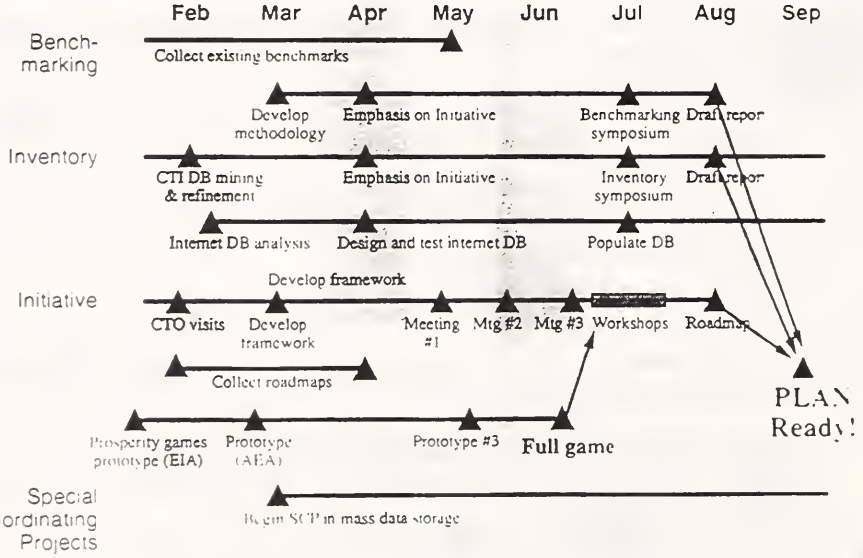
Draft schedule to turn the vision into a plan



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Long-Range ESC Goal

When any business, anywhere in the world, confronts a decision on where to locate, be it for research, design, manufacturing, or service, the clear choice is the USA because we have both the best environment for business and the best environment for life.

This will result in Jobs, Competitiveness, and Public Good.

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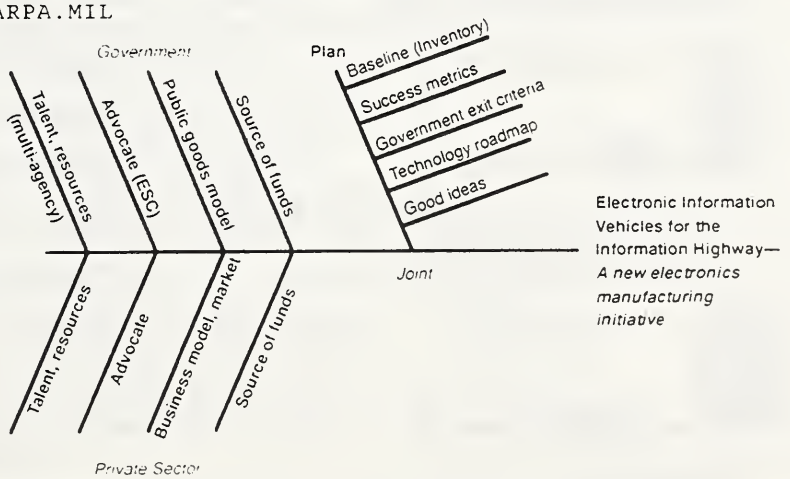
The ESC needs feedback

- Please send your comments to the Electronics Subcommittee, c/o ARPA/ESTO, 3701 N. Fairfax Drive, Arlington, VA 22203; or electronic mail: ESC@ARPA.MIL



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Backup

ESC

Visited or invited to participate in the NEMI Framework Process

Leading large and small companies intimately connected with the electronics industry:

Apple Computer Inc.
AT&T
Compaq Computer Inc.
Critical Technology Institute/RAND
Digital Equipment Corporation
Intel Corporation
IBM
Microsoft Corporation
Motorola
National Semiconductor
Philips Corporation
Silicon Graphics
Texas Instruments
Westinghouse
Xerox

ESC

Why the Federal Government is concerned with Electronics

- Competitiveness in electronics manufacturing is critical to the Nation
  - Largest U.S. manufacturing sector with 2.4 million American workers
  - Upstream of many key industries, e.g., computer, telecom, auto
  - Essential to National security
- There are major competitiveness issues facing the U.S. Electronics industry
  - Consistent bilateral trade deficit with Japan of $20B
  - 20% of total U.S. global trade deficit
  - U.S. global market and manufacturing shares dropping
  - New business challenges loom, e.g., green life cycle constraints, exploding capital equipment costs, shrinking product lifetimes, increased corporate networking
  - New technology challenges loom, e.g., new technology drivers
- Government must work with the private sector to facilitate long-term U.S. leadership and economic competitiveness in Electronics
  - The government has a role, whether it means to or not, through infrastructure, regulation, tax and trade policy, R&D investment, etc.
  - The ESC believes that the government can have a constructive role on competitiveness by
    - working in partnership with the private sector
    - investing in R&D and infrastructure
    - addressing policy issues

ref: AEA

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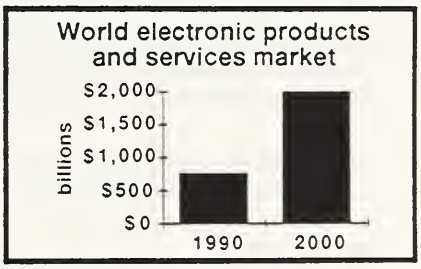
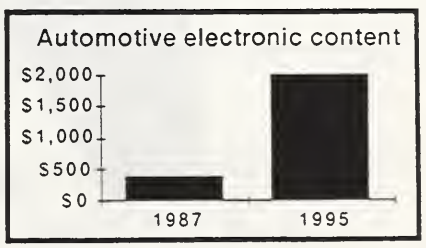
Electronics is Important to the Nation

- Electronics Industry was the largest industrial employer with 2,400,000 jobs in 1991
- It is the largest and the fastest growing U.S. manufacturing industry, projected to reach 25% of all U.S. manufacturing in 1995
- Electronics is key to competitiveness in other sectors such as Computer, Consumer, Telecom, Automotive, Aerospace, Chemical Process, and Medical





Sources: SEMATECH, NACS, EIA, DoD, AEA, Dallas Morning News

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We imposed a criterion of pervasive impact

Some of the Industries that Electronics impacts:

- Computer
- Telecommunications
- Education
- Automotive
- Entertainment
- Industrial Control
  (e.g., for Food and Chemicals, Buildings)
- Aerospace
- Consumer
- Medical
- Defense
- Environment

An electronics initiative should matter to and be engaged with a number of these customers. It must make a difference beyond just the electronics industry.

An Administration initiative should also be larger than what a single agency or the private sector can accomplish alone.

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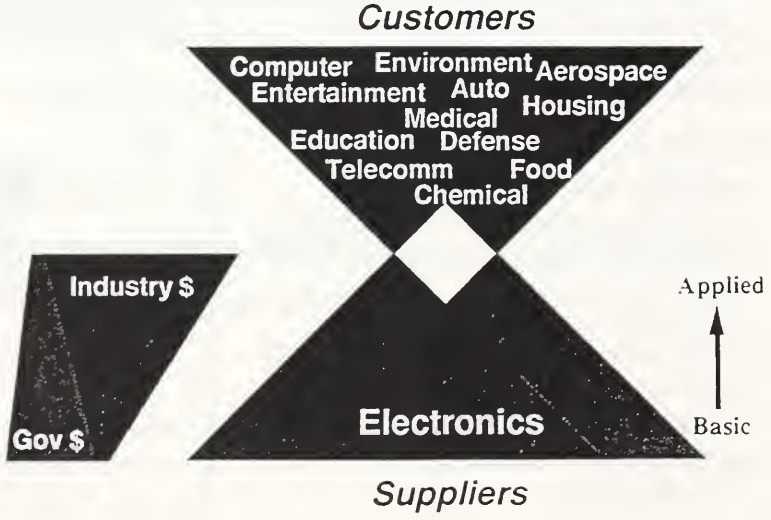
Focus the Tech Base on Customer Industries



ESC Discontinuities that will affect competitiveness in the information age

- There will be a revolutionary increase in information connectivity. For example, the wiring of the nation with cable and optical fiber and the work on HDTV are harbingers of these changes.
- There will be a revolutionary increase in mobile information services. For example, the explosion in cellular telephone usage and FCC actions on PCS (Personal Communication Systems) spectrum foreshadow even greater changes to come.
- There will be a revolution in innovation. Information devices are being redefined and resculpted in new and creative forms. Scanners are merging with photocopiers, cellular fax modems are being incorporated in portable computers, advanced automobiles are 30% electronics, TV is merging with personal computers, and new devices, such as the personal digital assistant, are coming on the market.
- There will be increasing emphasis on green manufacturing and life-cycle environmental considerations, including cradle-to-grave product management.
- Components are getting smaller and more sophisticated while demands for quality and low cost are increasing, making automated assembly more desirable than low-cost manual assembly.

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ESC Discontinuities, continued

- Customers are demanding more integrated products while companies are doing more outsourcing and networking. With more interfaces among companies, government effects on the business environment are even more important.
- Consumer electronics products are becoming technology drivers, often containing, and being manufactured with, the most sophisticated technologies.
- Developing countries will leap into new and modern infrastructures that will use advanced devices.
- Product development times and lifetimes continue to decrease as capital equipment costs explode. Risks increase.

Discontinuities provide the opportunity for make-a-difference investments

The right people; the right time; the right focus

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We have a vision for a focused Electronics Manufacturing Initiative

- Focus on electronic information products for the information highway
  - Will be a market and technology driver for electronics manufacturing over the next decade
  - Support Clinton Administration priorities, not only the National Information Infrastructure (NII), but also, potentially, the clean car, health care, and education.
  - Encompasses many of the technologies critical to success in all areas of electronics, e.g., packaging, semiconductors, displays, precision assembly, manufacturing, environmentally-conscious electronics manufacturing techniques; design for cradle-to-grave, batteries, robotics
- Government would provide support for enabling technology and infrastructure
  - Basic technology R&D. High risk investments for fundamental change.
  - Investments whose benefits private investors cannot hope to appropriate, but that a nation can.
  - Investments that serve a public need.
  - Infrastructure investment, e.g., Metrology. Machine tools and Equipment. Computer aids.
  - Technology deployment and extension services. Benchmarking.
  - Workforce education and training.
  - Mission-specific prototyping and procurement. (Defense, Education, Environment, etc.)
- Can deploy some existing government resources in FY94/95 (such as ATP or TRP) if the industry becomes enthusiastic and if a good plan is developed. On track to impact FY96 budget cycle.

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Said another way, the Electronic Information Vehicles for the Information Highway Initiative would be

- The basic product and process technologies
- Ranging from the fundamental to the applied
- For creating future world-class Electronic Information Products for the Information Highway
- Within a customer context supplied by nationally important industry clusters
- Consistent with key public goods such as education, health, environmental consciousness, and national security
- With government investments that can make a difference over the long term
- In partnership with the private sector

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Marshall Andrews, ITRI

ITRI

INTERCONNECTION
TECHNOLOGY
RESEARCH
INSTITUTE

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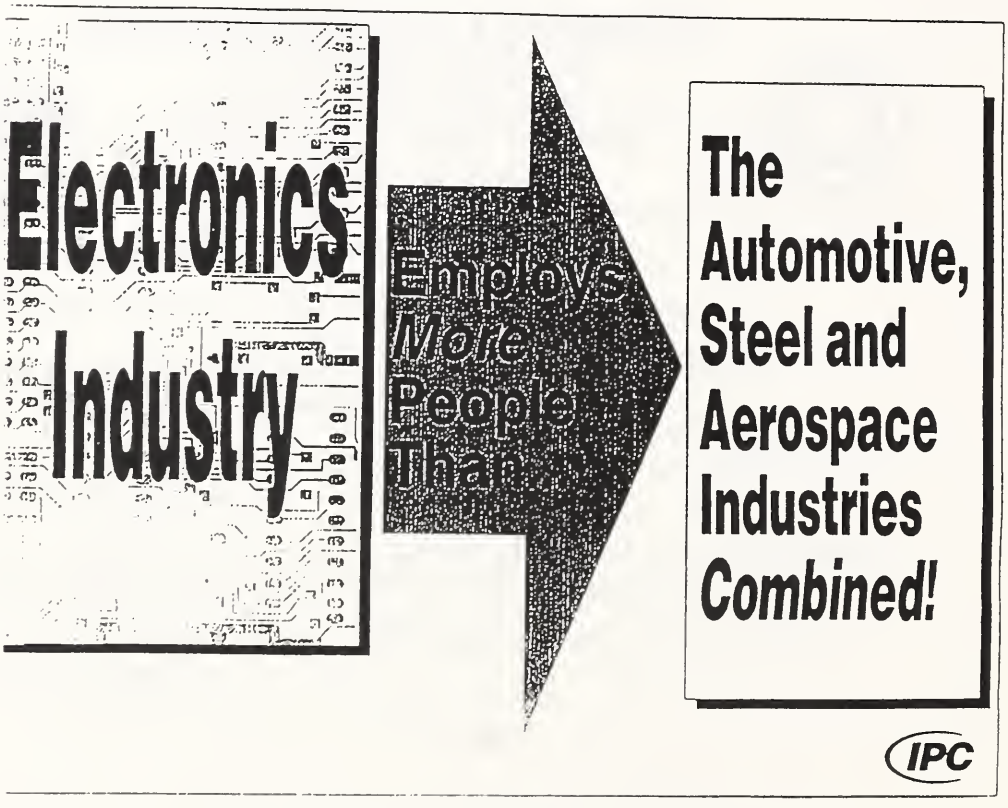

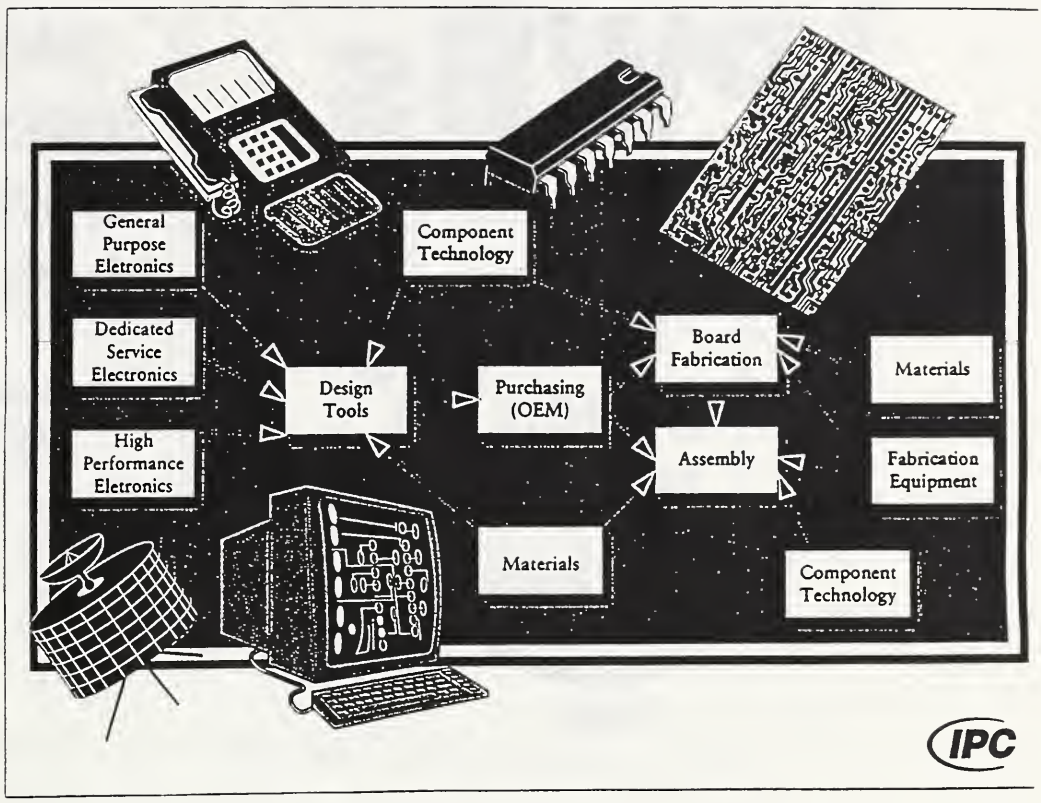

U.S. PWB and Assembly Industry

PWB Manufacturing

- 5.9 Billion in Sales Annually
- Over 100,000 Jobs, Including Those of Industry Suppliers

Including PWB Assembly

- 12 Billion in Sales Annually
- 200,000 Jobs in U.S.

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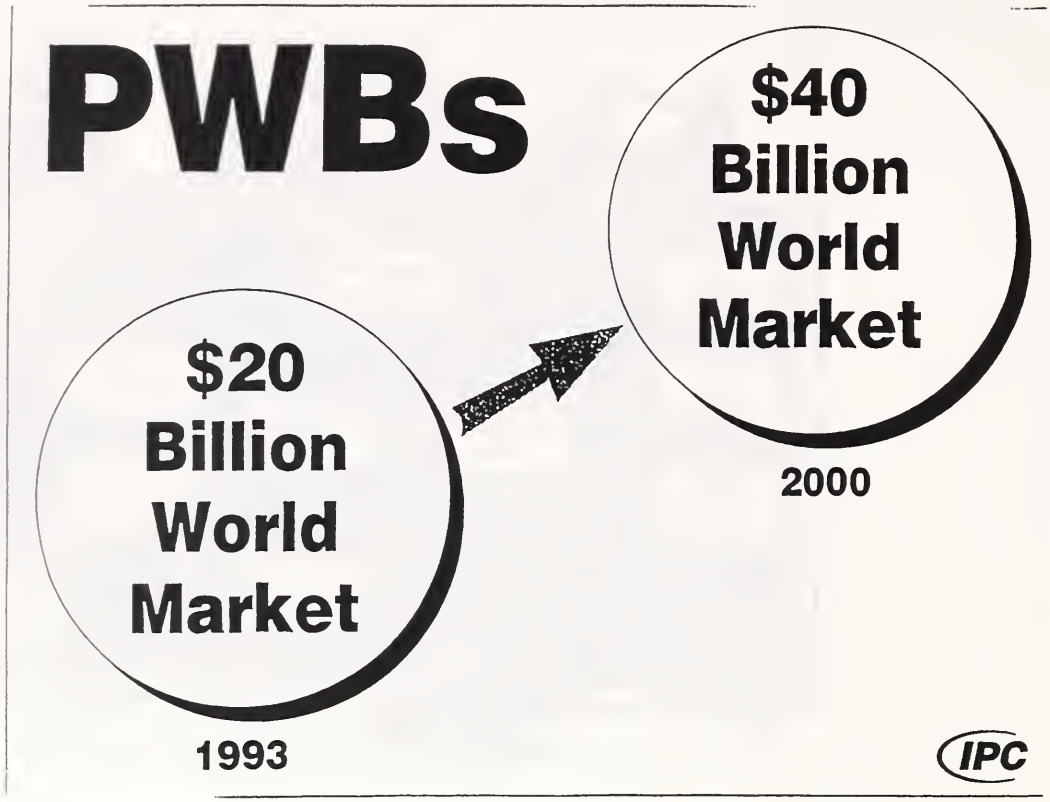
PWBs
$40
Billion
World
Market
2000
$20
Billion
World
Market
1993
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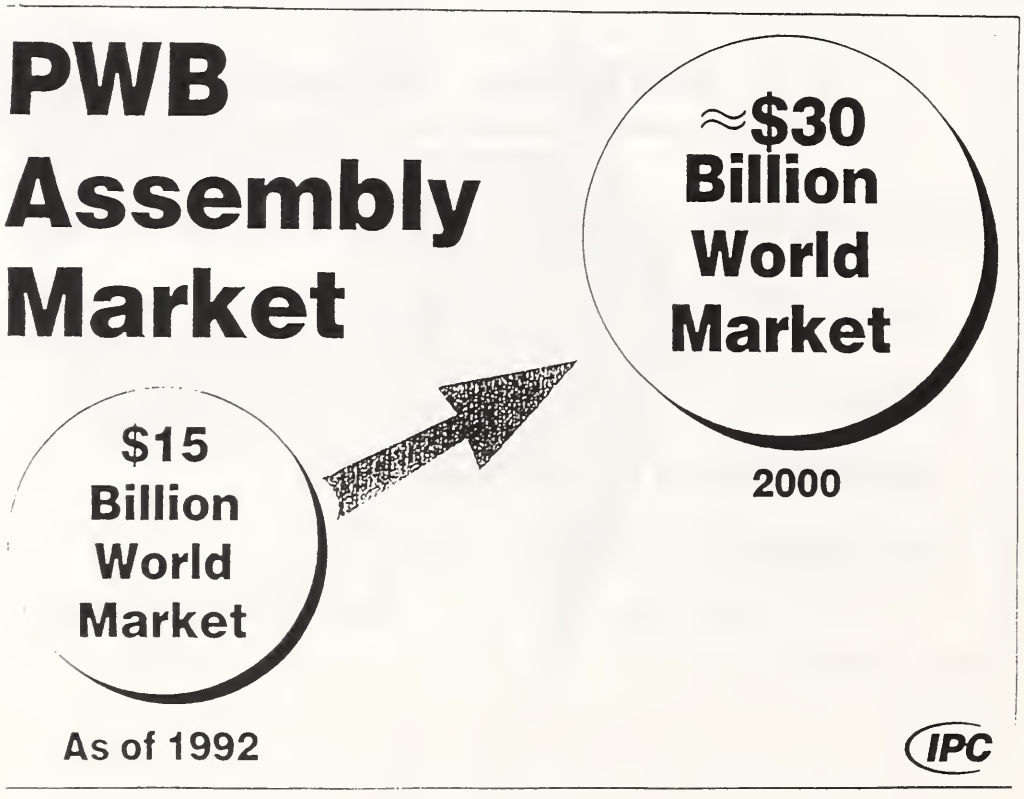
PWB
Assembly
Market
≈$30
Billion
World
Market
2000
$15
Billion
World
Market
As of 1992
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"Electronics will be one of the highest growth industries in the world in the next two decades."

Advanced Manufacturing Technology Initiative—U.S. Electronics Industry Priorities

American Electronics Association • August 1993

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"The U.S. must regain its competitive edge in a number of other strategic electronic system elements and their related material and equipment technologies, if it is to become the world leader in the electronics manufacturing industry."

Advanced Manufacturing Technology Initiative—U.S. Electronics Industry Priorities

American Electronics Association • August 1993

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Six electronic system elements are widely recognized for having the greatest impact on the U.S. electronics industry.
(In order of priority:)

1. Integrated Circuits
2. *Printed Wiring Boards (PWB) and Multichip Module (MCM) Substrates*
3. Liquid Crystal, Flat Panel Displays
4. Semiconductor Packaging Technology
5. *Printed Wiring and Substrate (MCM) Assembly Technology*
6. High Density Batteries

Advanced Manufacturing Technology Initiative—
U.S. Electronics Industry Priorities

American Electronics Association • August 1993

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Electronic Components

Technology	U.S. Position: Strong	Competitive	Weak	Losing Badly* or Lost
Microelectronics		●		
Electronic Controls		●		
Optoelectronic Components			●	
Electronics Packaging & Interconnections				●
Displays				●
Hardcopy Technology			●	
Information Storage	●			

* *U.S. Industry is no longer a factor or is not likely to have a presence in the next five years. It will take considerable effort or a major change in technology for the U.S. to become competitive.*

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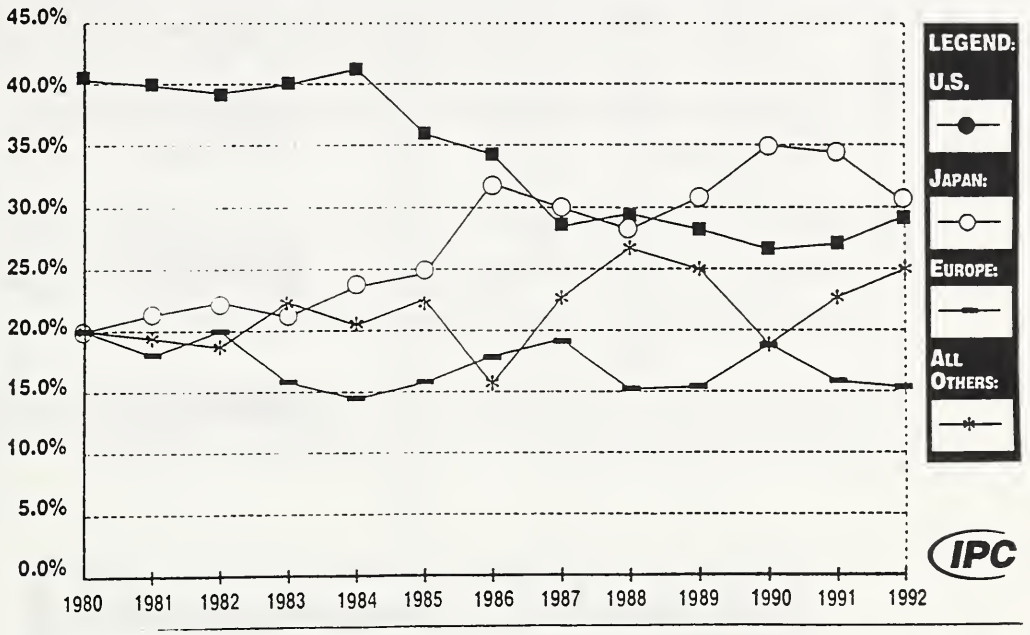
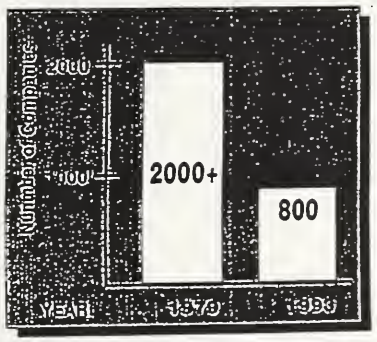
Historical World Market Share for Rigid and Flexible Circuits



U.S. PWB Industry

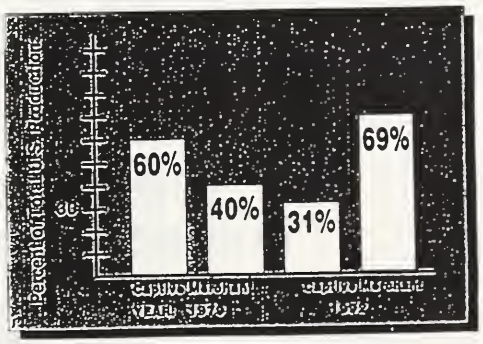
Trends in Industry Structure

90% of Independent PWB Manufacturers have annual sales of < $10 Million.



Low margins make capital investments difficult. Expenditure on R & D assumed to be decreasing with the trend toward outsourcing by OEMs.

Who will do the R & D necessary to regain competitiveness of this critical U.S. Industry?



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Printed Wiring Boards & Printed Wiring Assembly

Critical Technology for the United States

- PWBs and PWBAs are pervasive in electronics—not much you can do electronically without the PWB.
- Provide the interconnection between advanced ICs and humans.
- Multi-use technology is a major component of most electronic systems: computers, communications, automotive, military, industrial and consumer.
- Coming up on the screen as a major showstopper and critical technology for U.S. electronics industry.

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Competitive Requirements

- **PWB and PWBA Research and Development to find less costly ways to make interconnection products**
- **U.S. Leadership in Supporting Infrastructure Industries and Technologies**
  - PWB Fabrication Materials
  - PWBA Assembly Materials
  - MCM Substrate Materials
  - PWBA Assembly Equipment
  - PWB Fabrication Equipment
  - PWB Test and Inspection Equipment
- Volume Manufacturing Capability

Competitive U.S. PWB and PWBA Industry

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Premise

The U.S. must be a leader in PWB and PWBA technology and production, in order to be competitive in the world market for electronic systems.

Japan recognizes PWBs and PWBAs as critical technology and has, and is continuing to invest.

Manufacturers, suppliers, users and government must team if the U.S. is to regain competitiveness in this critical technology.

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We Need a National Strategy for PWB and Assembly Industry—
We Need a National Initiative...

ITRI

INTERCONNECTION TECHNOLOGY RESEARCH INSTITUTE

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ITRI MISSION

To enable revolutionary innovation and solutions for future requirements through improvement of existing technology, and development of advanced technology in manufacturing, materials and processes required to ensure a world class U.S.-based manufacturing capability for PWBs and PWB assembly that is environmentally responsible and cost effective.

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WHY ITRI?

- Unifying force for a fragmented industry providing a management structure which ensures all viewpoints are represented
- U.S. Jobs
- PWB is the heart and soul of electronic products

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WHY ITRI?

- The current system and method of industry R & D is inefficient.
- Allows industry and government to leverage R & D expenditures—cost effective R & D in a low margin, but critical industry.
- Valuable, proven approach to regain competitiveness.
- Tremendous possibilities if we can get several layers of supply chain in the industry working together.

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Vision of Success

U.S. PWB and PWB assembly industries become net exporters.

Globally competitive, environmentally benign technological leadership for the U.S. in interconnection products.

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FOCUS

Fostering partnerships among U.S. manufacturers, suppliers, customers and government to make a quantum leap in providing a cost effective interconnection module (assembled board).

For Today and Tomorrow!

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GOALS

- Develop environmentally benign manufacturing, materials and processes.
- Seek significant reduction in the total cost per square foot of interconnect systems.
- Develop manufacturing, materials, and processes necessary for high-volume production of high-yield, low-cost MCM-L.
- Develop methods that prove performance for advanced technology products/methods by which industry source materials do not require inspection and testing upon receipt.

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GOALS

- Improve performance of materials in their intended usage environments.
- Develop/define alternative materials to improve selected performance measures beyond the capabilities of those currently in use.
- Improve methods by which quality of process materials is determined.
- Improve current materials processing methods and operations to reduce cost, eliminate waste, and improve quality.

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GOALS

- Define/develop alternative materials processing methods and operations.
- Transfer new technology to manufacturers through IPC and other appropriate means.
- Achievement of other priorities identified in the Technology Roadmap for the Future of the Electronic Interconnection Industry.

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ITRI Objectives

- Regain Technological Leadership from Japan
- Regain Tactical Leadership from the Rest of Asia
- Viable, Competitive U.S. Industry
- Results Dissemination/Technology Transfer (Broad)
- Standards and Benchmarks
- World Class Quality

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Approaches

Strategic

The industry roadmap is the guiding force—all suppliers take integrated approach to change.

Operational

Change the *way* we do things to improve quality and reduce cost.

Market May Solve Issues

Tactical

Fabricators drive evolutionary change in existing technology—lower risk, quicker results

Revolutionary

Radical new approach—alternative materials or conceptually different process

High risk, long lead time—beyond scope of single company

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ITRI Philosophy

- Industry-led, public/private partnership
- Non-profit, non-manufacturing, virtual organization
- Consortium to administer funds for pre-competitive R&D
- Work closely with others—cooperation, not competition—whole supply chain involved
- PWB, flexible circuits and PWB assembly technology
- Work prioritized by industry technology roadmap
- Broad industry commitment and support—participation ***open*** to all interested U.S. companies

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ITRI Approach

- Phased approach based on prioritized needs with flexibility to take advantage of unforecasted opportunities—IPC Technology Roadmap
- Technical Council and Science Advisory Board
  - Evaluate needs and proposals
  - Organize workshops/project teams
  - Substantiate and recommend proposals for grant awards

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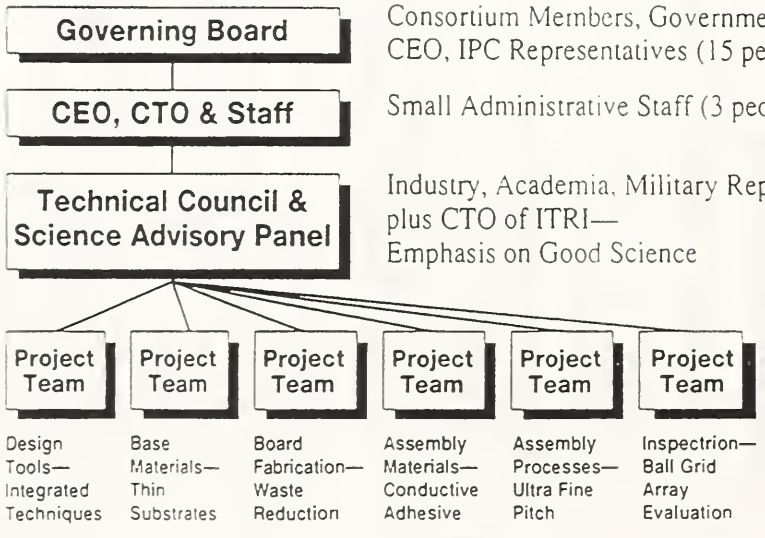
ITRI Approach

- Project Teams
  - Develop project mission, define work plan, specify outcome and document work
  - Once formed, teams control additions to the team and work effort
  - Project management
  - Majority U.S. owned
  - Major R & D resources in the U.S.
  - Committed to making the required financial contribution in cash or in kind

ITRI Operating Structure



PT Leadership: Each headed by a council member or consortium member company.
PT Membership: Any member company contributing to the project.

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ITRI Project Selection Criteria

- Relative Criticality of Need—Fits the Roadmap
- Size of Gap between Current and Required Performance
- Time Needed to Achieve Results
- Environmental Impact
- Technical Merit of the Approach
- Solutions are Cross-Disciplinary

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Where do projects come from?

- IPC Industry Technology Roadmap
- IPC Technical Committees
- ITRI Members
- Academia and Government
- Non-ITRI Members in Industry
- Other Groups

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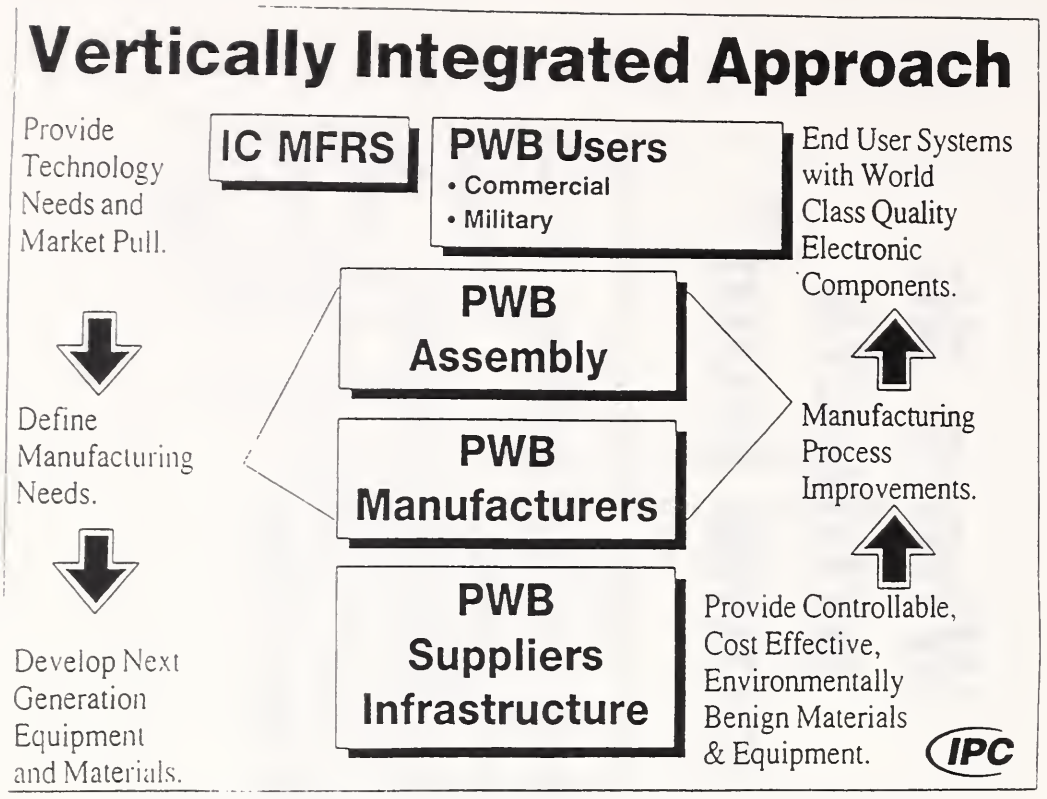
Vertically Integrated Approach
Provide Technology Needs and Market Pull.
IC MFRS
PWB Users
• Commercial
• Military
End User Systems with World Class Quality Electronic Components.
PWB Assembly
PWB Manufacturers
PWB Suppliers Infrastructure
Define Manufacturing Needs.
Manufacturing Process Improvements.
Develop Next Generation Equipment and Materials.
Provide Controllable, Cost Effective, Environmentally Benign Materials & Equipment.
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ITRI
Deliverables
• Legal structure for sharing—antitrust protection under National Cooperative Research Act
• Development of common needs of the industry
• Survival/growth a key segment of the U.S. electronics industry
• Solutions to industry problems—today and tomorrow
• Opportunity for consortia project participation/leadership
• Reduced costs in manufacturing
• Reduced cost, higher ROI on industry R & D
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ITRI Deliverables

- Information on ongoing ITRI projects—quarterly progress reports and final technical report for each ITRI project/program
- Workshops for developing detrailed work statements for each project—allowing for participation by any member
- Right of first refusal for all new equipment, materials and processes to member companies
- Opportunity for active role in industry benchmarking activities

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Critical Mass

- Company Commitment to Participate—Three Years
- Government Commitment to Partnership
- CEO and CTO Selected
- IPC Committed Initial Funding Necessary to Create Critical Mass

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ITRI Funding

Membership Fee

Sales	Contributions
<$5 MM	$1,000
$5 – 10 MM	$2,500
$10 – 50 MM	$5,000
>$50 MM	$10,000

Covers Overhead and Administration

Private or Joint Government/Private Funding of Individual Consortium Projects/Programs

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MICHAEL SCHEN, NIST

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TECHNOLOGY PARTNERSHIPS WITH NIST

Michael A. Schen
Materials Science and Engineering Laboratory
National Institute of Standards and Technology
Gaithersburg, MD 20899

for the

Workshop on
Materials Metrology and Data for Commercial Electrical and
Optical Packaging and Interconnection Technologies
Hilton Hotel, Gaithersburg MD
May 6, 1994

NIST

NIST R&D PROGRAM IN ELECTRONIC PACKAGING AND INTERCONNECTION MATERIALS

- May 1990 Workshop crystallized NIST R&D planning for expanded program in electronic packaging and interconnection.
- Focus on metrology for measurements of properties of materials and materials structures.
  - Well aligned with NIST's historic role
  - Supports oft-neglected national infrastructure
  - Generic precompetitive nature
  - Broadly applicable across the industry
- Supplements Prior Efforts in Design and Manufacturability of Packaging Systems (Thermal Control, Wire Bonding, Hermeticity, Electromigration)

NIST

NIST R&D PROGRAM

- Program Focus:
  packaging issues at and above the chip level
- Program Scope:
  processing, inspection methods, properties data, performance measurements, and improved materials and tests for... substrates, encapsulants, adhesives, solders, conductors, and interconnects
- Program Goals:
  develop techniques and procedures for making in-situ measurements on materials and structures having micrometer and sub-micrometer dimensions

  quantify and record the divergence of material properties from their bulk values as dimensions are reduced and structures are confined

  standardize measurements on materials and material structures

  disseminate materials properties data in a form that can be used by the microelectronics industry

NIST

PROJECTS IN PACKAGING AND INTERCONNECTION

Computerized Information Exchange via STEP, Joe Carpenter (301.975.6397)
developing and implementing standards for the computerized exchange of digital data consistent with the International Organization for Standardization (ISO) program called STEP (STandard for the Exchange of Product data model) for electronic packaging materials

Micromechanical Measurements, David Read (303.497.3853)
developing micromechanical measurement techniques for the measurement of elastic modulus, yield and ultimate strength, and elongation to failure of metal thin films and developing experimental mechanics techniques to verify analytical predictions by direct observation of local displacements, strains and stresses

Dimensional Stability of Polymers, Michael Schen (301.975.6741)
joint development of measurement techniques, protocols, and standard reference materials with electronics packaging materials suppliers and users for coefficient of thermal expansion (CTE) and dimensional change due to absorption of moisture

Cure Monitoring in Electronic Packaging, Tom Davis (301.975.6728)
developing means of assessing performance of polymer films and layers by developing methods of measuring the conversion of polymer precursors to final layers and developing methods for measuring influence of cure on polymer properties most significant to electrical performance and interfacial integrity

Polymer Process Monitoring, Fred Mopsik (301.975.6747)
developing dielectric and capacitance methodologies for polymers as processing and inspection methods, for properties data, performance measurements and improved materials for the substrates, encapsulants, and conductors used in electronic packaging and interconnects

NIST

PROJECTS (continued)

Mechanism of Adhesion of Polymers, Wen-Li Wu (301.975.6839)
developing a fundamental understanding of the parameters important in interface debonding and the role of environmental agents, such as water, on the interfacial stability of thin polymer films used in packaging on an Angstrom scale using neutron and x-ray reflectivity

Self-Reinforced Packaging Composites, Barry Bauer (301.975.6849)
developing and applying concepts in advanced interpenetrating polymer networks to the synthesis and characterization of self-reinforced polymeric resins with improved thermal, mechanical, and dimensional control

Electromagnetic Characterization of Electronic Interconnects, Roger Marks (303.497.3037)
developing methods to electrically characterize interconnections by measuring very high frequency (GHz) transmission line properties, impedances, and scattering parameters using microwave instrumentation and seeks to define the fundamental parameters and procedures for conducting accurate measurements

Solderability Measurements and Optimization, John Manning (301.975.6157)
developing new measurement techniques for solderability based on improved understanding of surface wettability and reactions at solder-substrate interfaces leading to new accelerated tests for determining component solderability after tinning

Lead-free Solders, Carol Handwerker (301.975.6158)
developing tools for understanding and evaluating solderability, determining phase diagrams, and measuring the mechanical properties of environmentally safe alternatives for lead-based solder alloys in conjunction with the National Center for Manufacturing Sciences (NCMS)

NIST

NIST Proposal: *THE ADVANCED PACKAGING AND INTERCONNECTION MATERIALS METROLOGY FORUM*

- A NIST-wide forum for building industry collaborations and broadly leveraging NIST results within the U.S. electronic packaging and interconnection and material supplier industries
- Help bridge the gap between material suppliers and microelectronic device manufacturers and users
- Focus on improvements in materials measurement science and data quality / availability to support goals in commercial microelectronic packaging established by U.S. industry
- Vehicle for accelerating development, standardization, and implementation of improved metrology
- Utilize CRADAs to protect intellectual property and assign rights

NIST

JOHN GUDAS, NIST

NIST

Advanced Technology Program

John P. Gudas

Technology Administration
Department of Commerce

NIST UNITED STATES DEPARTMENT OF COMMERCE
National Institute of Standards and Technology
DR. JOHN P. GUDAS
Program Manager for Advanced Materials
Advanced Technology Program
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Gaithersburg, MD 20899
Office (301) 975-3214
Fax (301) 926-9524
gudas@micf.nist.gov

THE FEDERAL ROLE IN TECHNOLOGY

- How is the government investing in science and technology?
  - Total U.S. R&D > $150 B / year
  - Federal government provides 45% of the funds for U.S. R&D
    - » 60% for defense, mostly weapons system development
    - » 15% for health
    - » 0.5% for industrial development

- What has changed?
  - Global competition has accelerated the rate of innovation and challenged U.S. industry
  - Post Cold War ⇒ opportunity to refine our technology investment strategy

THE FEDERAL ROLE IN TECHNOLOGY

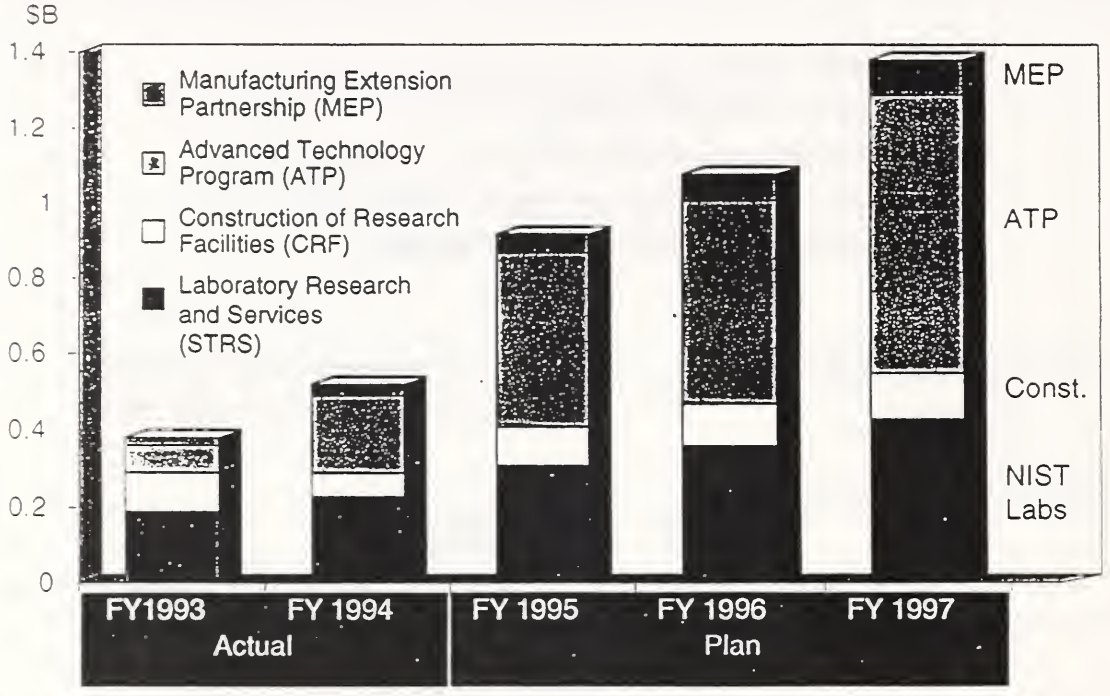
- How is the government responding to change?
  - Invest in civilian technology
  - Drive defense toward a dual-use technology base
  - Transfer technology from government labs
  - Continue commitment to basic science

NIST MISSION

- To promote U.S. economic growth by working with industry to develop and apply technology, measurements, and standards.

NIST OUTYEAR SUMMARY

President's Plan



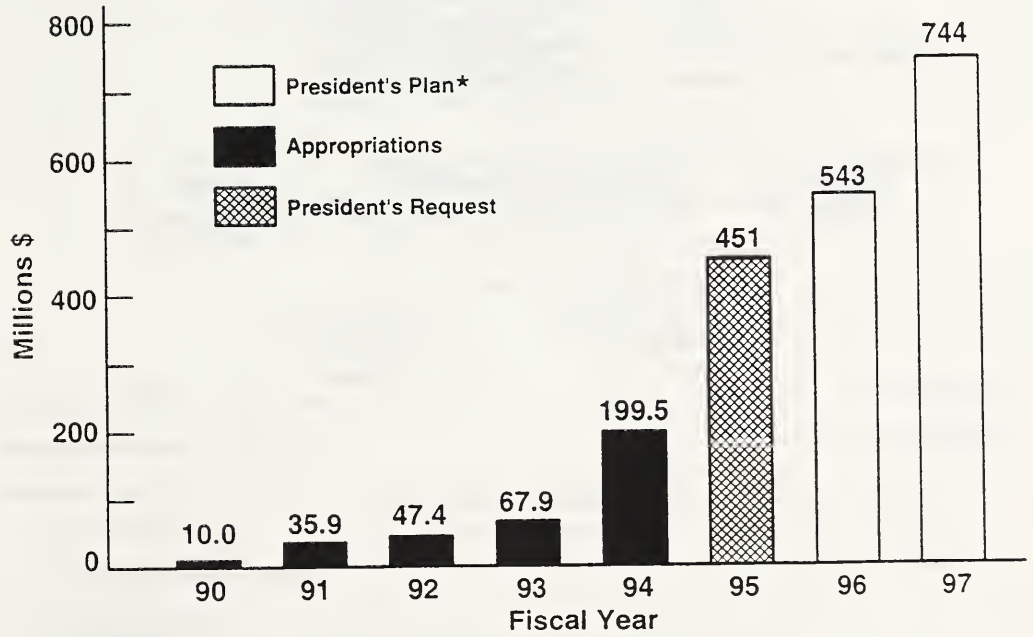
ATP MISSION

- Stimulate U.S. economic growth by developing high-risk and enabling technologies through programs proposed and cost shared by industry

BASIC CHARACTERISTICS

- Unique mission focus - - high-risk enabling technology development to stimulate U.S. economic growth
- Partnership with industry - - industry conceives and proposes ideas, executes and cost-shares projects; ATP applies selection criteria
- Focused and general competitions - - for depth and breadth
- Competitive selection process - - technical and business reviews
- Sunset provisions - - for both programs and projects
- Performance metrics - - for both process and programs

ATP BUDGET PROFILE

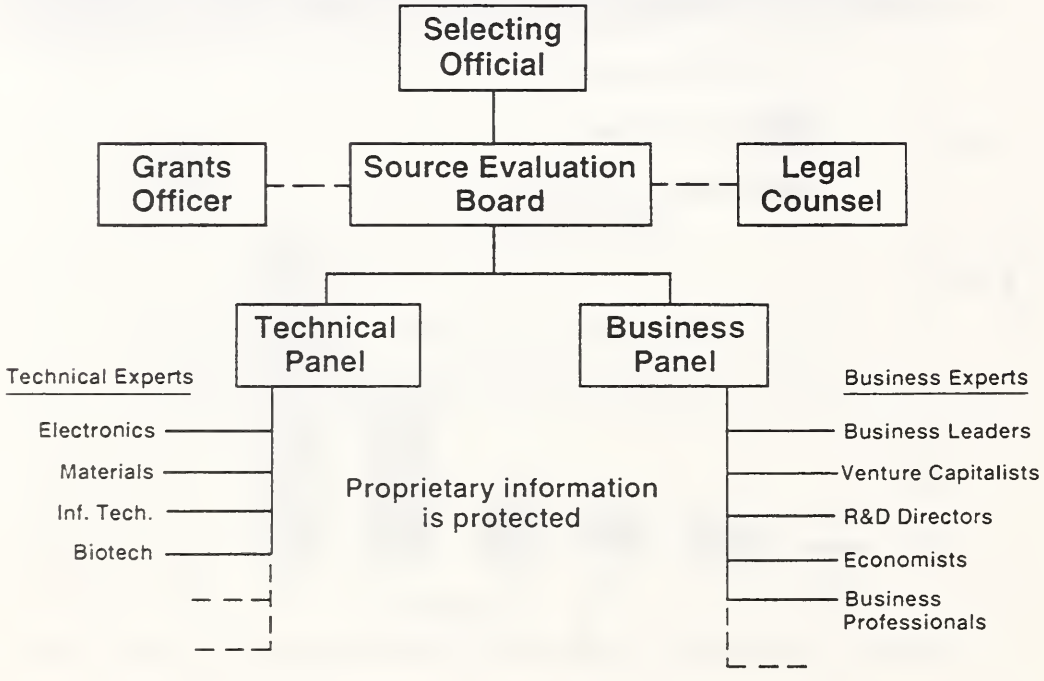


* Based on "A Vision of Change for America," President Clinton's Economic Plan - - February 17, 1993

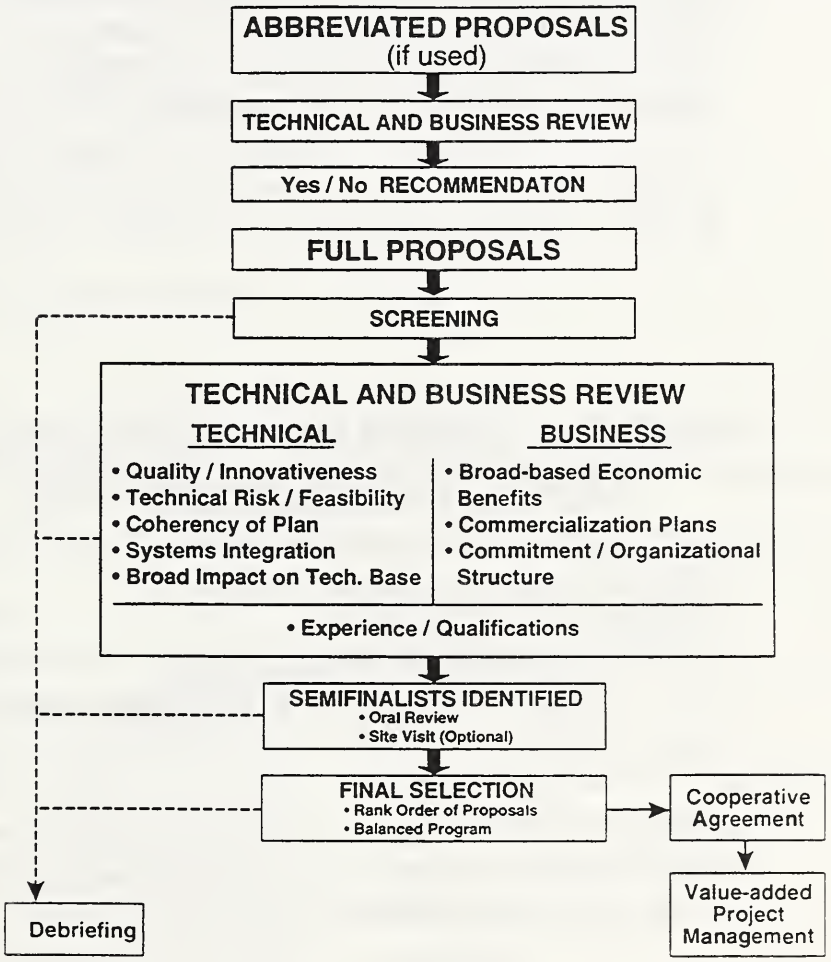
ATP ELIGIBILITY

- Individual companies
  - No more than 3 years
  - Up to $2M total
  - NIST pays only direct costs
- Joint ventures
  - No more than 5 years
  - No limit on award amount
  - NIST share less than 50%
- No direct funding to universities, government agencies or non-profit independent research institutes

SELECTION PROCESS MANAGEMENT



ATP PROJECT SELECTION PROCESS



INTELLECTUAL PROPERTY PROVISIONS

- Companies incorporated in the U.S. keep intellectural property rights
- Companies can license
- Government reserves the right to a royalty-free non-exclusive license for government use
  - Non-disclosure (trade secrets protected)
  - Government rights rarely invoked

FOREIGN COMPANY PARTICIPATION

- Project must result in economic benefits to the U.S.
  - R&D and manufacturing in the U.S.
  - Increase U.S. employment
  - Promote U.S. supplier infrastructure
  - U.S. - owned companies also must meet these requirements
- Country of origin must grant opportunities to U.S. - owned companies comparable to any other company in that country and protect intellectual property
- PL 102-245 authorizes suspension of award if criteria no longer satisfied

FOUR GENERAL COMPETITIONS

ATP STATISTICS

Proposals Submitted	912
Participating Organizations*	1352
Total ATP Funding Requested	$1.5 B
Total Estimated Cost-Share	$1.5 B
Number of Awards	89
(Joint Ventures)	(23)
(Single Applicants)	(66)
Participating Organizations*	200
Total ATP Funds Committed	$247 M
Total Estimated Cost-Sharing	$268 M
Award Size - - Range (ATP Funds)	$500 K - $20 M

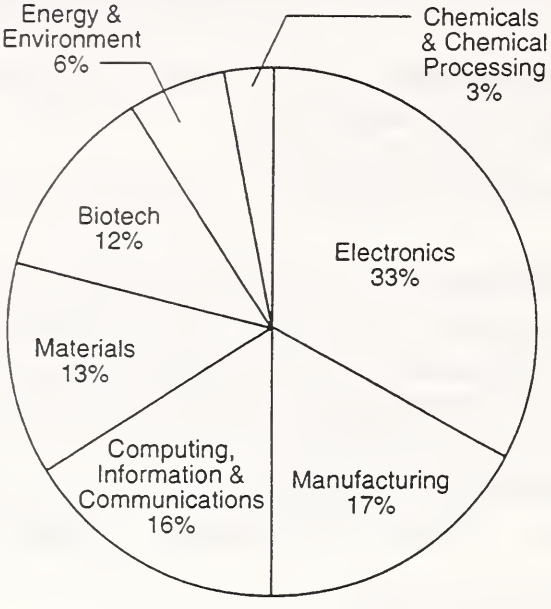
* Excludes Subcontractors

ATP TECHNOLOGY AREAS

- Machine Tools
- Image Recognition & Processing
- Semiconductor Processing
- Genetic & Tissue Engineering
- Flat Panel Displays
- Lasers, Optics & Electro-optics
- High Performance Computers
- Optical Communications
- Ceramics, Composites, & Polymers
- Automated Mfg. & Robotics
- Motor Vehicle Assembly
- Plastic Recycling
- Superconductors
- Energy Conservation & Distribution
- X-ray Lithography & Optics
- Optical & Magnetic Storage
- Printed Wiring Boards
- Illumination

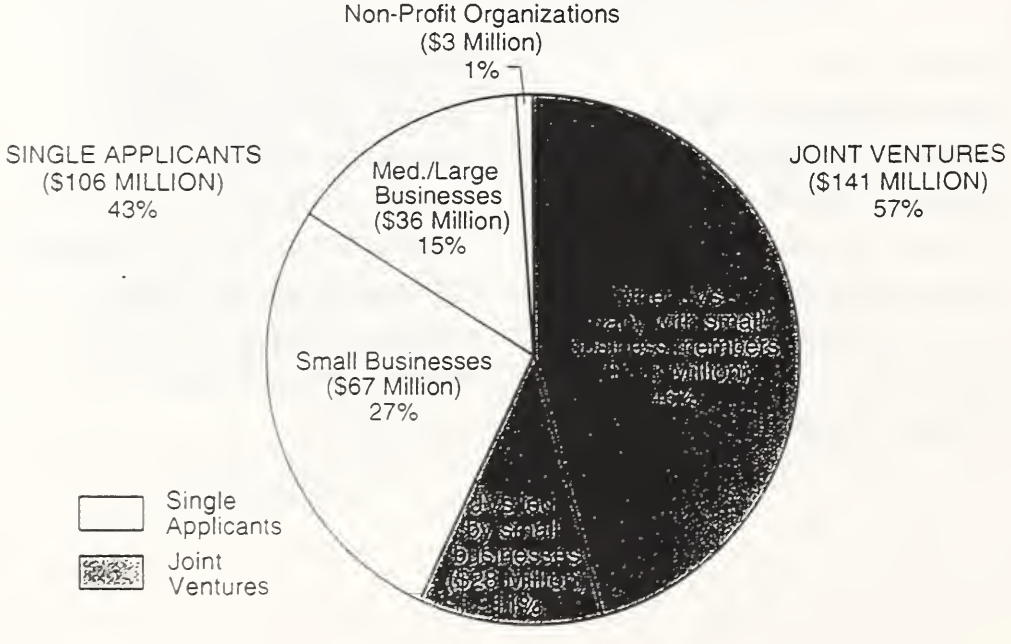
FOUR GENERAL COMPETITIONS

TECHNOLOGIES FUNDED BY ATP
AS A PERCENT OF $247 M AWARDED



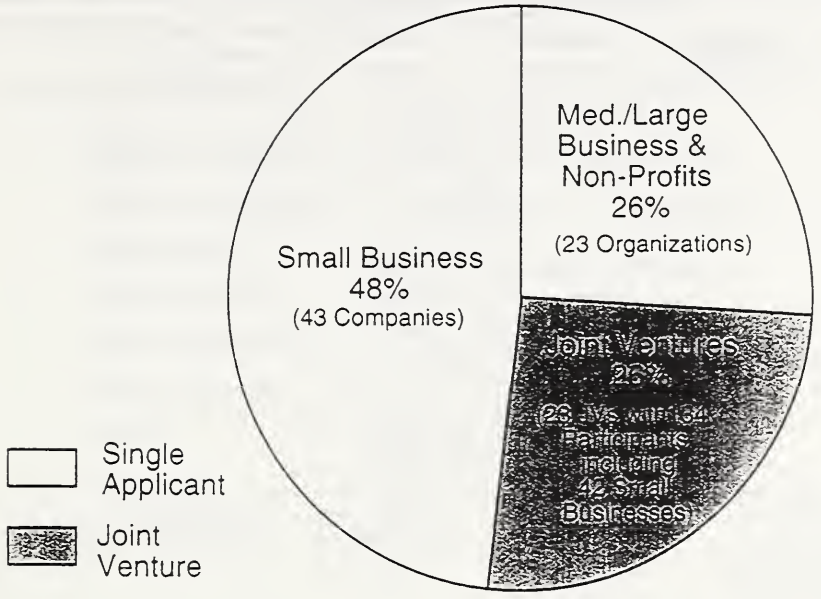
FOUR GENERAL COMPETITIONS

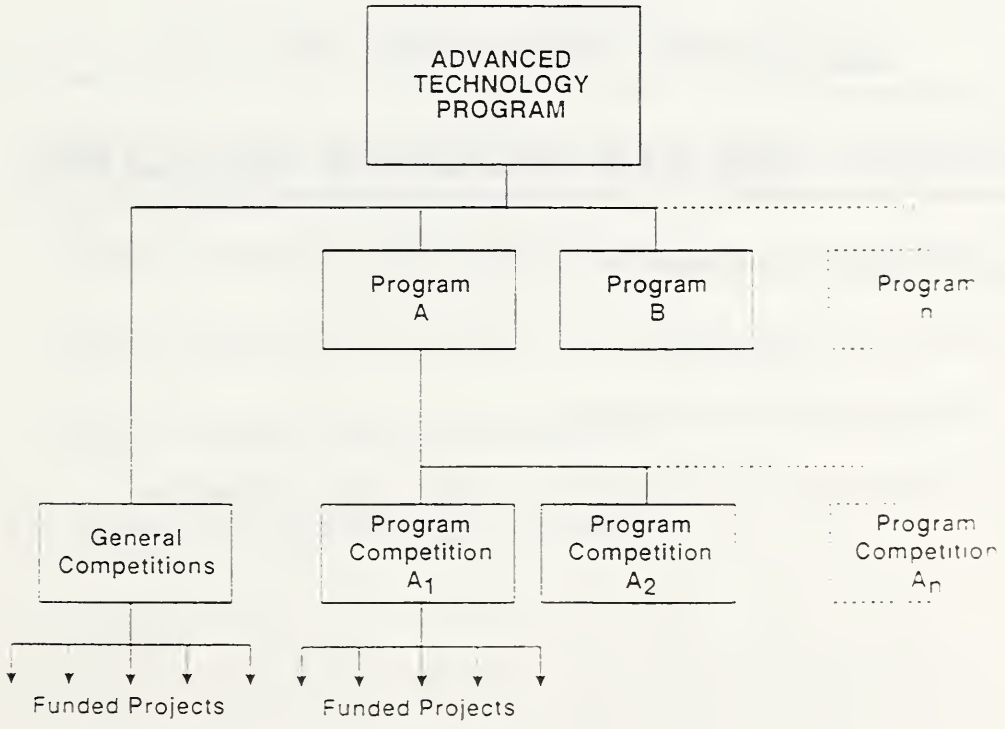
$247 MILLION OF ATP FUNDS AWARDED
BY TYPE OF ORGANIZATION


Non-Profit Organizations ($3 Million) 1%
SINGLE APPLICANTS ($106 MILLION) 43%
JOINT VENTURES ($141 MILLION) 57%
Med./Large Businesses ($36 Million) 15%
Small Businesses ($67 Million) 27%
Single Applicants
Joint Ventures

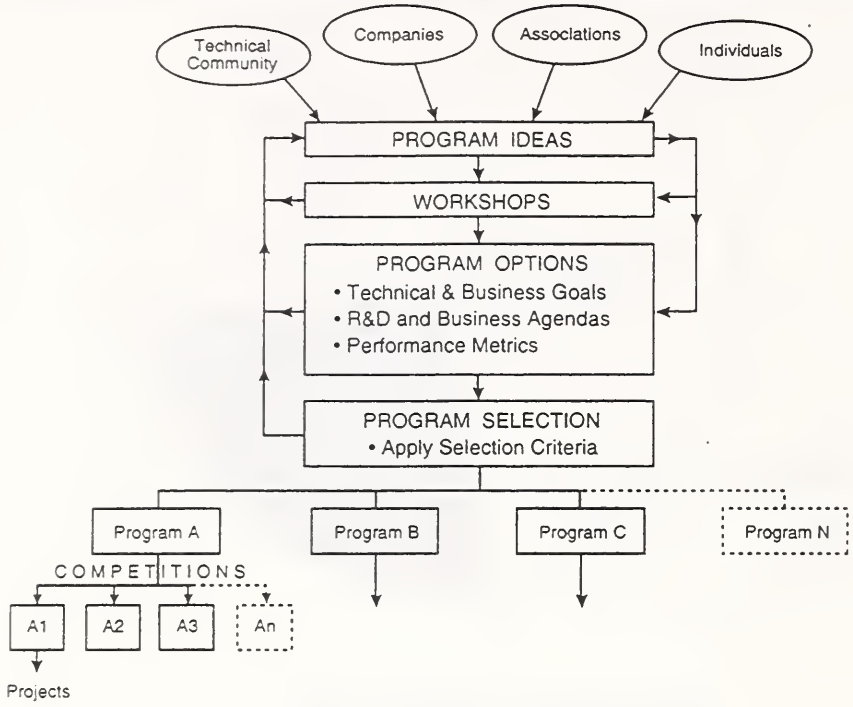
FOUR GENERAL COMPETITIONS

ATP 89 AWARDEES
BY TYPE OF ORGANIZATION





PROGRAM PLANNING, SELECTION AND EXECUTION



CRITERIA FOR ATP PROGRAM SELECTION

1. Potential U.S. economic benefit
2. Good technical ideas
3. Strong industry commitment
4. Opportunity for ATP funding to make a major difference

PROGRAM IDEAS RECEIVED
(Through February 1994)

- 550 submissions - - ideas still coming in

Biotechnology	51	Chemical	18
Communications	31	Construction	12
Electronics	64	Energy	29
Environment	25	Food	12
Instrumentation	10	Manufacturing	54
Mass Storage	7	Materials	68
Optics	15	Packaging	21
Services	14	Software	73
Transportation	29	Other	17

FY 1994 FOCUSED PROGRAMS

- 94-02 Manufacturing Composites Structures
- 94-03 Computer-integrated Manufacturing for Electronics
- 94-04 Healthcare Information Infrastructure
- 94-05 Tools for DNA Disgnostics
- 94-06 Component-based Software

ATP MEASURES OF SUCCESS

Longer Term Measures:

- Rates of Return on Investment (Private, Public, and Social)
- Aggregate Employment Effects
- Sales and Value added
- Manufacturing Costs / Product Quality / Time to Market
- Market Share (U.S. and International)
- New Industry Creation
- Multiple-Use Technology Creation

Contacts:

ADVANCED TECHNOLOGY PROGRAM

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Nicholas Naclerio, ARPA

March 29, 1994

Enhancing the Competitiveness of U.S. Electronic Packaging Industries

1. Introduction

On October 29, 1993, President Clinton requested the National Economic Council (NEC) and the National Security Council (NSC) to develop a strategy to improve the competitiveness of the electronic packaging industries in the United States. To undertake this effort, the NEC and NSC coordinated an interagency initiative involving the Departments of Defense, Commerce, and Energy; National Aeronautics and Space Administration (NASA); the U.S. Trade Representative; the Office of Management and Budget; the Council of Economic Advisors; and the Office of Science and Technology Policy. This paper represents the first step in articulating a national vision and an action plan for electronic packaging.

2. Packaging Technology and its Role in the Electronics Industry

Electronic packaging is the science and art of establishing interconnections and a suitable operating environment for electronic circuits. A package generally contains a number of circuit components combined into a functional unit or module. The four major functions of the package are:

- circuit protection
- signal distribution
- power distribution
- thermal management.

Circuit protection involves mechanical support and protection from physical damage as well as protection from environmental hazards such as moisture, contaminants, or ionizing radiation. Signal distribution involves creating well characterized electrical connections between various components in a module and providing interfaces to the next level of assembly. Power distribution involves the distribution and conditioning of the electrical current necessary for the integrated circuits (ICs) to function. Thermal management is necessary to remove heat generated by the electronic components so that they stay within an allowable temperature range.

Electronic packaging is a critical element of a competitive electronics industry. All electronic systems use some type of electronic packaging. For high end systems such as supercomputers and mainframes, packaging is a primary determinant of system performance; for compact, portable electronics, it is a primary determinant of size and weight; and for almost all electronic systems, it is a primary determinant of reliability. The assembly of a complete system generally involves several levels of packaging. This report focuses primarily on the first-level of packaging, the enclosures protecting individual integrated circuits and other electronic components. Subsequent levels of packaging provide interconnections among the IC modules and may involve printed circuit boards (PCBs), card cages, backplanes, and cabling. For the remainder of this report, semiconductor packages and electronic packaging will be used interchangeably to refer to first-lovel packaging.

Semiconductor packages are fabricated out of a number of different materials, primarily plastic, ceramic, and metal. Metal packages are primarily used for discrete transistors and small integrated circuits requiring only a few leads. They are also used for military hybrids and some high frequency applications where the metal package provides electromagnetic shielding for the device. The complexity of passing leads through the conducting metal body of the package without shorting makes extendibility to higher lead counts difficult.

Ceramic packages are typically used for applications requiring high reliability, high thermal dissipation, or operation in harsh environments. Examples include defense and space systems, leading edge microprocessors, and some industrial electronics. They are generally manufactured by a supplier, who provides the completed packages to the semiconductor manufacturer or contract assembler for incorporation of the integrated circuit and final sealing. Ceramic packages simplify device reliability since the package does not come in contact with the active surface of the device and, when hermetically sealed, is completely impervious to moisture, air, and ionic contaminants that can harm the IC. The materials used in ceramic packages also offer a high degree of thermal conductivity, making them useful when the IC dissipates more than a few watts or is to be used in a high temperature environment.

Plastic packages are used for nearly all other applications due to their small size and low cost, generally one half to one tenth the cost of comparable ceramic or metal packages. In 1992, approximately 98% of all integrated circuits were packaged in plastic. Plastic packages are usually constructed by injecting a molding compound into a form that already contains the semiconductor device attached to a metal lead frame. Improved materials and processes allow manufacturers to make plastic packages that are only slightly larger than the integrated circuit die and which can be used reliably in most environments. The thermal performance of plastic packages can be enhanced by adding metal heat spreaders or heat slugs, but this decreases their cost advantage over other types of packages.

Most semiconductor packages house a single IC, however, most circuits consist of multiple ICs interconnected on a Printed Wiring Board (PWB). An alternative to integrating a number of Single Chip Modules (SCMs) on a PWB is to integrate a number of "bare" or unpackaged ICs into a single first-level package called a Multi-chip Module (MCM). A slight variation, called chip-on-board, involves attaching the "bare" or minimally protected chips directly to a printed wiring board, eliminating the first-level of packaging altogether. Both approaches yield substantial gains in performance, density, and reliability and are currently being used in high performance systems, compact consumer products, and some military applications. There are several different approaches being used to implement MCMs which evolved from different technology bases. Laminated MCMs (MCM-L) are manufactured using a process derived from PWB manufacture. Deposited thin-film

MCMs (MCM-D) are manufactured using processes similar to semiconductor manufacturing. Ceramic MCMs (MCM-C) are manufactured using the same process as single-chip multi-layer ceramic packages. All three types of MCM technology are competitive for certain mid-range applications although MCM-L is generally considered the least expensive and MCM-D is generally considered the highest performance and density. MCM-C has advantages for some high power applications and applications requiring hermeticity. Elements of the three approaches are sometimes used in combination to satisfy multiple requirements.

3. Trends in Packaging Technology

While performance, size, cost, and reliability are important for all types of packaging, there are two distinct sectors of the semiconductor packaging market. One is driven primarily by size and cost reduction and the other is driven by performance enhancement. While the two are currently following different technology paths, there is a convergence in their long term trends.

For most semiconductor products, the drivers for semiconductor packaging are smaller, thinner, lighter, and cheaper. These include memory cards, consumer electronics, and portable telecommunications applications. These applications are primarily implemented in single-chip, plastic packages. According to the Semiconductor Industry Association's (SIA's)15 year technology roadmap for packaging, these applications are likely to migrate to smaller, thinner plastic packages, chip-on-board (COB), and simple multi-chip modules (MCMs). To minimize board or MCM area, bare chips will eventually be attached face down to pads directly beneath them using a process called "flip-chip". This eliminates any area or height that would have been taken up by the package or leads and reduces the amount of packaging materials consumed.

At the other end of the product spectrum are high performance microprocessors and Application Specific Integrated Circuits (ASICs). While only a few percent of total IC unit sales, these products are driving higher clock speeds, increased lead counts, and greater power dissipation. To meet the requirements of these important, high margin products, the package must provide shorter, more controlled electrical paths, shorter, more conductive thermal paths, and much greater number of interconnects between ICs. The new Ball Grid Array (BGA) package, offering shorter electrical paths and requiring less board area, will likely be used for many of these applications. Again the SIA roadmap predicts a migration to flip-chip, and high performance MCMs throughout the remainder of the decade. Flip-chip allows the maximum number of signal connections because they can cover the entire surface of the chip; it also provides the shortest possible electrical path. MCMs allow the chips to be placed very close together and provide high quality signal routing between chips. The elimination of the single chip packages means that the back of the integrated circuits can be directly contacted for heat removal.

These two discontinuities in the technology evolution may create an opportunity for new players to enter the merchant packaging market. Various estimates place the size of the MCM market at between $800 million and $8 billion by the end of the decade. It should be noted, however, that these new technologies are not likely to completely displace existing packaging approaches for at least the next decade due to the substantial existing capital base.

4. Market Structure and Trends

Semiconductor packaging is done by semiconductor manufacturers or their contract assemblers. In the case of plastic, this means purchasing the molding compound and lead frames, attaching the integrated circuit to the lead frame, and molding the package around the IC and lead frame. In the case of ceramic packages, metal packages, or MCMs; this means purchasing components and assembling them. Large systems companies may also specify and/or purchase single or multi-chip packages, especially when the MCM will incorporate die from multiple suppliers.

In 1993, the worldwide market for all packaging materials rose to $4.9 billion, according to market research firm Rose Associates. The largest segments of the current market (by value) are ceramic packages and the encapsulation resins and lead frames used to make plastic packages. (Because of their higher cost, ceramic package materials make up a larger fraction of total materials sales than their unit volume would suggest.) The following chart shows the growth in materials sales between 1988 and 1993.

Worldwide Materials Consumption ($ millions)

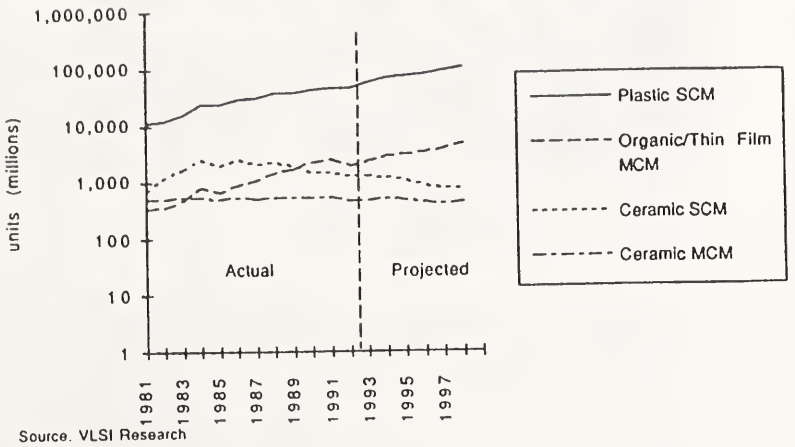
	1988	1993	1996 (forecast)
Ceramic Packagage Materials (CERDIP & Metallized Ceramic Packages)	1,436	1,340	1,560
Plastic Packages Materials (encapsulation resin & leadframes)	1,540	2,395	3,140
Other Packaging Materials (bonding wire, seal lids, die attach, headers & cans, hybrid materials, other)	1,232	1,177	1,397
Total	$4,208	$4,912	$6,097

Source: Rose Associates

The increase in consumption of materials for plastic packages relative to the other materials categories is due to improvements in plastic package reliability and

performance which have enabled most high volume products to use plastic. The following chart shows the actual and projected volume by package type.

Worldwide Unit Demand by Package Type



Source. VLSI Research

Shown on a logarithmic scale, the strong growth in plastic packages and Organic/Thin Film MCMs is apparent. The decline in unit volume for ceramic packages is due primarily to the decline in demand for CERDIPs, simple pressed ceramic packages used for certain types of memories and simple military ICs. The loss in sales revenue from CERDIP packages is offset by increased sales of Ceramic Pin Grid Arrays (CPGAs), a much more expensive type of multi-layer ceramic package used for microprocessors and ASICs. CERDIP production facilities are generally not convertible to CPGA production, which requires a multi-layer ceramic process.

There are a number of other materials that are used for all types of electronic packages. They include die attach adhesives, wire bond wire, Tape Automated Bonding (TAB) materials, metal cans, and lids. The markets for these materials range from a few tens of millions of dollars to a few hundreds of millions of dollars. Like the materials for plastic and ceramic packages, the absolute size of the markets for these materials understates their importance to the electronics industry.

Defense Markets

The Department of Defense (DoD) and other government agencies are not significant purchasers of packaging materials. Rather, they acquire electronic systems that incorporate and depend upon already packaged integrated circuits. For reliability and reparability, government customers such as DoD and NASA often specify what types of packages their suppliers must use. Historically this has meant hermetic, ceramic packages. A new acquisition strategy being pursued by DoD that is based on best commercial practice will likely result in a mixture of both ceramic and plastic packages in future military systems. The Department of Commerce (DoC) estimated that the value of the ceramic packages purchased by defense suppliers in the U.S. was $107 million in 1992, down 6% from the previous year. This represents less than 9% of the total world market. Since the absolute value of defense purchases is likely to decline in coming years, the defense fraction of the total market is likely to diminish even further.

5. Current State of the U.S. Packaging Industry

To reduce costs, most semiconductor manufacturers have relocated their package assembly operations to low labor-cost regions, particularly in Asia. According to SEMATECH, 79% of assembly by U.S. IC manufacturers is performed offshore by a mix of captive and contract assembly houses. This relocation has probably contributed to the loss of market share by U.S. packaging equipment and materials suppliers. Between 1984 and 1992, U.S. assembly and packaging market share fell to 10% from 12% for materials and to 31% from 39% for equipment. In 1993, there were no U.S. companies in the top ten world suppliers of packaging materials, and only one U.S. equipment supplier was in the top ten.

The relatively low priority placed on packaging is probably a reflection of the markets U.S. semiconductor companies have targeted. The majority of all ICs produced by U.S. semiconductor companies go into the computer, telecommunications, and automotive market segments. In those sectors, form factor has not been a primary product differentiator, and for most products performance was not package limited. On the other hand, Japanese semiconductor companies are much more closely tied to the consumer electronics marketplace where cost, size and weight are the primary drivers. As a result, they hold the lead in compact low cost packaging.

At the very high end, where packaging is a performance limiter, the U.S. has maintained technology leadership, although the majority of production is performed by captive suppliers. This captive production is important from the point of view of national competitiveness since it supports substantial R&D, contributes to the strength of lower tier suppliers, and represents substantial technical know-how. For example, the DoC found that in 1992, captive production of ceramic packages represented roughly 87% of domestic production value ($431 million of $498 million) which in turn represents roughly 30% of global production value. Captive producers support over half of all commercially funded R&D. Total domestic production

represents 41% of domestic consumption. On a unit basis, however, total domestic production of ceramic packages is small compared to Japanese production levels.

The merchant market for ceramic packages is currently dominated by four Japanese companies. In 1992, Kyocera, NTK, Shinko, and Sumitomo supplied approximately 92% of the world-wide merchant market, with Kyocera alone providing over 58%. Furthermore, the DoC found that U.S. merchant producers are heavily dependent upon foreign suppliers for raw materials and manufacturing equipment. According to the DoC report "domestic customers rate Japanese suppliers to be superior on a wide range of competitive factors including: breadth of product line, historical performance, quality, and service." Between 1988 and 1992, U.S. merchant vendors increased their aggregate market share to 7% from 4%. This increase in market share was due to increased sales of multi-layer ceramic packages.

Market share for plastic packages is slightly more complex since the packages are not purchased as discrete components, but rather formed by the semiconductor manufacturer or contract assembler from materials usually purchased from suppliers. The two main elements of a plastic package are a metal lead frame, which is stamped or etched by the supplier into a particular pattern for each IC type, and an epoxy resin molding compound. The merchant markets for lead frames and plastic molding compounds are also dominated by Japanese suppliers. The top two molding compound suppliers are Japanese and do not produce any product in America. According to SEMATECH, the total market share of U.S. based suppliers fell to 15% in 1992 from 20% in 1989. During the same period, U.S. suppliers' market share for lead frames increased to 15% from 11%. The top five suppliers of lead frames are all Japanese and manufacture all of their product abroad.

Preliminary results from a recent government sponsored study on electronic packaging in Japan, finds the Japanese ahead in 11 of 15 aspects of electronic packaging production, parity in one aspect (wire bond) and a U.S. lead in only three (MCM-D, flip-chip assembly, and design). In two of the 11 areas that Japan leads in volume manufacturing, single and multi-chip ceramics, the U.S. leads in basic technology, but lags in high volume, low cost production capability.

Packaging Technology Assessment - United States vs. Japan

	Technology	Volume Mfg. Product Application
• Single Chip Modules		
Plastic	Japan	Japan
Ceramic	U.S.	Japan
• Multi-Chip Modules		
Thin Film (MCM-D)	U.S.	U.S.
Ceramic (MCM-C)	U.S. (High Performance)	Japan (Low Cost)
Laminate (MCM-L)	Japan	Japan
Chip-on-Board (COB), Chip-on-Glass (COG)	Japan	Japan
• Chip Assembly		
Flip-chip	U.S.	U.S.
TAB	Japan	Japan
Wire Bond	Parity	Parity
• Package Assembly (Process, Tools, Density)	Japan	Japan
• Passives, Components	Japan	Japan
• Printed Wiring Board (PWB)	Japan	Japan
• Flex Circuits	Japan	Japan
• Connectors (elastomeric, anisotropic)	Japan	Japan
• Design	U.S.	U.S.

Source: Japanese Technology Evaluation Center at Loyola College

Changes in end-product markets mean new requirements for semiconductor packages. The evolution of the computer and telecommunications industries towards portable, hand-held products means that size and weight will become increasingly important. Increases in semiconductor device performance mean that packaging may become a performance limiter for common desktop computers. The combination of these trends means that electronic packaging will increasingly become a product differentiator for mainstream devices produced by U.S. semiconductor companies.

Recent Developments

• A number of new merchant suppliers of advanced packaging solutions have emerged in the U.S. and appear to be winning new business from older packaging

technologies. These companies, primarily focused on MCM-D technologies, are recognized as global technology leaders in this emerging market.

• Less than one year after entering the merchant market, IBM has begun producing commodity CPGA packages and has reportedly entered into a number of important OEM supplier relationships. Increased internal and external orders have caused IBM to increase production rates from last year.

• SEMATECH, working with SEMI/SEMATECH, established a Standardized Supplier Qualification Assessment (SSQA) and a Technology Assessment Protocol (TAP) for ceramic package suppliers. The adoption of these methodologies by the SEMATECH membership will greatly reduce the effort required by companies who wish to become qualified to supply multiple U.S. semiconductor companies with packaging materials. One supplier audit has already been completed and a second is being initiated.

6. Government Support for Packaging Technology R&D

The federal government funds over $150 million of packaging related R&D annually. About three quarters of this money goes directly to the U.S. industry through contracts, grants, and other agreements. The remainder is spent in government laboratories on programs that usually involve industry collaboration. Approximately 85% of those funds go towards projects that are dual use in nature and directly aid the competitiveness of the domestic infrastructure. Many of the projects involve cooperative activities and are cost-shared with industry. Below is a breakdown of the FY94 funds by agency.

	FY94 ($M)
DoC/NIST	6
DoD/ARPA	112
DoE	32
NASA	5
Total	$155

The funding is targeted at a range of packaging approaches including single-chip modules, multi-chip modules, and printed circuit boards as well as a range of support technologies such as design tools, assembly equipment, testing, reliability, metrology, and advanced materials. The support technologies are generally independent of packaging approach and materials approach and make up over 40% of the federal investment. Projects range from basic research through application demonstrations in commercial and military systems.

Of the 60% of federal R&D that is invested in specific packaging approaches, roughly two thirds is directed towards performance driven applications. Examples include critical military functions such as automatic target recognition, command and control, and precision strike as well as important commercial applications such as high performance computing, high speed networking, and automatic test equipment. Technologies under development include thin-film multi-chip modules, optical interconnects, 3-D packaging schemes, microwave packaging, and new materials and systems for thermal management. Also under development are new packaging technologies aimed at compact, light weight, low cost solutions for applications such as personal navigation, wireless communications, and hand-held computing. These technologies include low-cost laminates, mixed signal packaging, and adhesive flip-chip. The objective in all of these programs is to develop healthy domestic suppliers who can satisfy both defense and commercial requirements.

7. A National Strategy for Electronic Packaging Technology

Access to leading edge electronic packaging technology is important to the health of the semiconductor and electronics industries in the United States. Changes in end-product markets mean new requirements for semiconductor packages. The evolution of the computer and telecommunications industries towards portable, hand-held products means that size and weight will become increasingly important. Increases in semiconductor device performance mean that packaging may become a performance limiter for common desktop computers. The combination of these trends means that electronic packaging will increasingly become a product differentiator for mainstream devices produced by U.S. semiconductor and electronics companies.

The current state of the domestic electronic packaging industries creates cause for concern. Measured in terms of market share or technological leadership, the U.S. industry lags behind the market leaders in many important areas such as the high volume production of multi-layer ceramic packages, laminate multi-chip modules, and small, thin plastic packages.

The U.S. leads the world in packaging technologies for very high performance systems such as mainframe computers, telecommunications switches, and military systems. As semiconductor device performance increases, high performance packaging will be needed for an increasing number of products ranging from workstations and personal computers to engine controllers and digital high definition television. Substantial public and private investment have led to new technologies that have the potential to address the needs of these new markets. However, without a presence in the high volume, low cost production of current generation packages, the U.S. may have difficulty capitalizing on these new packaging approaches.

Any strategy to strengthen the competitiveness of the U.S. electronic packaging industries must include support and participation from both the packaging industries and the semiconductor industry, the primary customers for the product. The semiconductor industry depends upon the health of its supplier infrastructure. By agreeing to common requirements, setting priorities, and collaboratively investing in the long term health of its supplier base, the semiconductor industry can reduce the suppliers' cost of doing business and benefit from lower prices and more capable suppliers. Government can play a role in facilitating and supporting this process.

The government can support the industry by funding basic research and high risk technology development, as well as cooperating with industry to encourage the formation of industry-led teams to address pre-competitive technology challenges. The federal government is already investing over $150 million annually in electronic packaging R&D.

Government also plays a role as a major customer and beneficiary of advanced packaging technologies. As such, it may need to support the development of certain niche technologies of critical importance to the national defense or other public purposes that lack sufficient market size to sustain private investment. However, in most cases the government's needs as a customer are best met if they can be integrated with the needs of the rest of the marketplace and served by a healthy domestic industrial base.

Discontinuities taking place in the evolution of packaging technology and an increased focus on packaging by the principle customers present an opportunity for the U.S. to strengthen its competitive position in this important industry. To be successful, a highly focused and coordinated strategy is needed. The following action plan, developed in consultation with the semiconductor and packaging industries represents the first steps of that strategy. The plan builds upon ongoing federal programs, the Department of Commerce's previous recommendations regarding the ceramic packaging industry, and the Department of Defense's efforts to foster dual-use technologies and strengthen the national industrial base.

Action Plan

• The Administration will establish an interagency specialists' group to work with industry to develop a set of National R&D priorities and a technical roadmap that will lead to U.S. leadership in electronic packaging. The group will include representatives from the Departments of Commerce, Energy, and Defense, NASA, and the National Science Foundation, and report to the National Economic Council and National Security Council, as necessary. The group will be chaired by a representative of the Advanced Research Projects Agency (ARPA).

• The semiconductor industry, through SEMATECH, should take the lead in addressing near term industry packaging priorities. The government currently supports these activities through 50/50 cost sharing and will work with industry to allocate a portion of SEMATECH's budget to packaging that is commensurate with its priority to the industry.

• The Administration will support the expansion of the supplier qualification program established by SEMATECH to address all areas of electronic packaging critical to the semiconductor industry. Participation in the program should be open to all domestic suppliers who are sponsored by either a SEMATECH member or a government customer. This will both lower barriers of entry for new domestic suppliers and establish further opportunities for customer/supplier partnerships.

• The Administration will fund a new $30-40 million initiative to stimulate domestic packaging R&D in low cost electronic packaging. This initiative will complement ongoing government programs and seek to enhance U.S. competitiveness in key packaging technologies for high volume markets such as desktop information systems, automotive engine controls, and hand-held electronics. The interagency initiative will be led by ARPA and administered through the Technology Reinvestment Program (TRP). All packaging alternatives proposed by industry-led teams committed to high volume domestic manufacturing will be considered. Since the TRP requires matching contributions from industry, this initiative can be expected to lead to at least $60-80 million in new technology investments in this area.

• The Administration will continue to support ongoing federal R&D programs that are maintaining U.S. leadership in high performance packaging technologies as well as critical enablers such as design, test, and reliability. It will also continue support for basic materials and process R&D that are essential for long-term technology leadership.

• The Administration will work with industry to eliminate any artificial barriers between the defense and commercial markets. This will assure that U.S. vendors have maximum access to the defense markets and R&D and will allow the DoD and other government customers to take advantage of the economies of scale and increased efficiency provided by the commercial market.

8. Conclusions

Electronic packaging is, and will increasingly be, important to the competitiveness of U.S. semiconductor and electronics industries and to the national security. Advancements in semiconductor device performance have outstripped improvements in packaging technology. Desktop computers are now facing the same type of performance bottlenecks that were overcome with sophisticated packaging solutions on mainframes, but require solutions that are an order of magnitude less expensive. New automobiles, dependent upon electronics for engine control, braking, and collision avoidance, need electronics as reliable as that used in military aircraft. Portable, hand-held computing and telecommunications devices such as personal digital assistants and cellular phones are the fastest growing segment of the electronics industry. They require packaging technology that is compact and very low cost like earlier solutions for consumer products, but with added performance capabilities. These market changes mean that if the U.S. semiconductor and electronics industries are to maintain their leadership positions in global markets, they must have access to new packaging solutions. These technologies must offer the performance previously required only for super-computers with the compactness and low cost required by the consumer electronics industry and the reliability previously required only by the military. To maintain its leadership position in the global electronics marketplace and provide the foundation upon which to build the National Information Infrastructure, the U.S. must regain leadership in high volume low-cost production. Success will require a significant effort on behalf of U.S. industry and government. This action plan is a first step toward establishing an industry/government partnership to achieve those objectives.